A 250°C ASIC Technology

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Abstract

Tekmos has developed a 250°C ASIC technology that uses the X-Fab XI10 SOI process. A gate array architecture was chosen to allow reduced mask costs and quicker manufacturing cycle times. The design of the technology includes first determining the optimum routing grid and then designing of the basic gate array transistors. The "A" style transistor was chosen over the "H" style to create stronger transistors. The choice of the transistor in turn sets the characteristics of the basic "Block" that is used in the gate array architecture. Another factor in the block design is the requirement for a pre-determined source with "A" transistors. This prevents the use of shared diffusions that are used in most gate array architectures and resulted in a different block layout. The pre-determined sources also required a change to the logic cell library. Since the basic transmission gate found in most flop designs cannot be used, alternative logic architectures were developed. By implementing the SOI specific library into the Tekmos standard logic library, the SOI peculiarities were masked from the end designer. The 250°C ASIC technology was demonstrated in a FPGA conversion, in which a design in an Actel MX series FPGA was re-implemented in the 250°C ASIC technology. A standard FPGA design conversion flow was used, and the only issues were related to the speed and voltage differences between the FPGA and the 1.0µ ASIC. These were addressed through critical path analysis and some slight circuit modifications. The temperature derating for 250°C was significant, but enough margin was retained to allow the circuit to work. Parts were made and worked as expected at 250°C. The life testing results at 280°C have been satisfactory. On an experimental basis, parts were evaluated at temperatures of up to 305°C without failure.

Design Goals

The goal was to create a high temperature ASIC technology to be offered to the market as a general solution to 250°C operation. While others also provide high temperature solutions [1], Tekmos considered it important to develop the technology in a cost-effective manner that would shield design engineers from temperature related issues. Tekmos wanted to use its existing gate array methodologies and IP and have them work at 250°C.

Process Selection

The first step in developing a technology is to select the process, which is linked to the process vendor. A true SOI process was needed that was both available and did not have excessive mask charges. The 1.0µ, triple metal, SOI, XI10 process, offered by X-Fab [2] at their foundry in Erfurt, Germany, was chosen.

X-Fab also offers a combination of engineering lots and MLM (Multi-Level-Masks) that are well suited to the volume demands of most high temperature applications. X-Fab provides the layout rules, process specifications, and spice models that are the initial step in creating our new technology.

Transistor Selection

Each SOI transistor needs to have a substrate connection, and this connection needs to be within 3µ of any part of the channel. Otherwise, leakage currents could trigger bipolar activity which could cause circuit failure.

The substrate connection can either be part of the source ("A" style) or it can be connected through the gate overlap ("H" style). The "A" and "H" designations result from the resulting shape of the transistors, visible in Figure 1. The "A" style was chosen because it supports the creation of arbitrarily

large transistors. The layout problems, caused by having a pre-defined source with the "A" style, are discussed later.

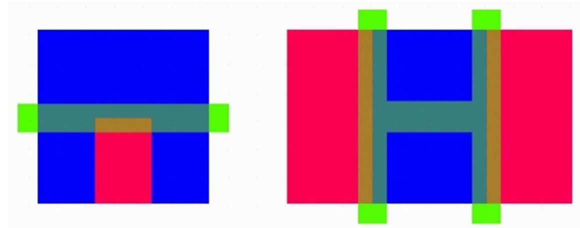

Figure 1. Layout of A and H transistors

Routing Grid and Block Design

The next step was to determine the routing grid and to specify a "block" of transistors that was compatible with the routing grid.

The "X" routing grid is typically a function of the Metal-3 layout rules, especially the spacing between adjacent vias. In this process an "X" grid of 4.4µ, was used.

The selection of a "Y" grid is more complex. Major considerations are the Metal-2 via spacing, the Metal-3 via spacing, the distance between two contacts on either side of a gate, and the distance between two contacts in separate diffusions.

Because the Metal-1 and contact rules are typically tighter than the higher metals, a design with off-grid contacts can be used to obtain a smaller grid, but at the expense of possible DRC errors when the entire circuit is implemented. A "Y" grid of 3.4µ was selected, using off-grid source contacts.

A transistor width was selected. In general, increasing a transistor width also increases the load presented by the next stage and results in no speed advantage. Increasing the transistor width does, however, change the ratio between interconnect capacitance and gate load. With larger gate to interconnect ratios, fewer buffers are needed to compensate for routing delays. This advantage must be balanced against the increase in power consumption caused by the larger transistors. A transistor width of 12µ was chosen. (There is a note on these choices in the Conclusions section.)

Another transistor width choice is between P and N transistors that are electrically equal, and those which are physically equal. Asymmetry in electrical strength can be useful in critical timing situations and physical symmetry assists in routing. This project used P and N transistors of the same physical size.

The transistors are typically grouped together into a block (Figure 2) that is then repeated to form the array of gates.

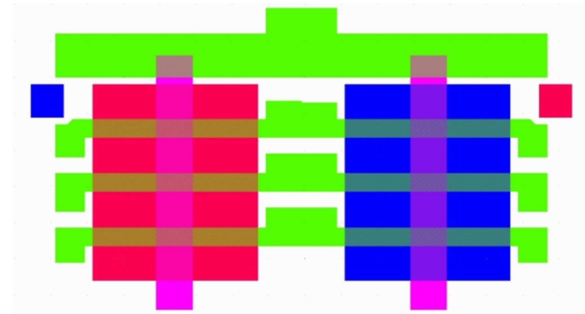

Figure 2. Typical Gate Array Block. Red=P, Blue=N, Green=Poly, Magenta=Metal-1 Power.

Type "A" transistors, with dedicated sources prevent the use of multiple pairs of transistors in a block. Instead, a design with a single transistor pair in each block was used. (Figure 3) The inability to share source and drains within a block lowered the overall gate density to 928 gates / mm^2.

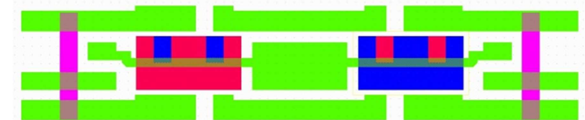

Figure 3. SOI Block

The requirements for the "A" style transistors require that the sources be populated with contacts and metal. This blocks a number of prospective Metal-1 routing channels, complicating the implementation of primitive cells entirely on, or below, the Metal-1 layer. The purpose of this design constraint was to allow the Metal-2 and Metal-3 layer completely available for interconnect.

This problem was solved by providing a small amount of poly interconnect in each block for the connection of the sources to the supplies, the

connection of the P and N channel drains, and the creation of a poly tunnel under the Metal-1 supply buses for cells that were multiple columns wide. To address concerns about the inclusion of the poly resistances effecting timing, a post processing step was added that shorts out the poly interconnect sections that are not covered by Metal-1 routing.

Flip-Flop Transmission Gates

Most logic gates translate directly into an SOI technology. One device type that does not translate is the transmission gate typically used in flip-flops and latches. The sources and drains of transmission gates are interchangeable, a characteristic unavailable with the use of "A" type transistors.

The solution chosen was use of a pair of clocked inverters as a replacement for the transmission gate, as shown in Figure 4. This makes the flops larger, though the size increase can be offset by incorporating the inverter functions into the design of the rest of the flop.

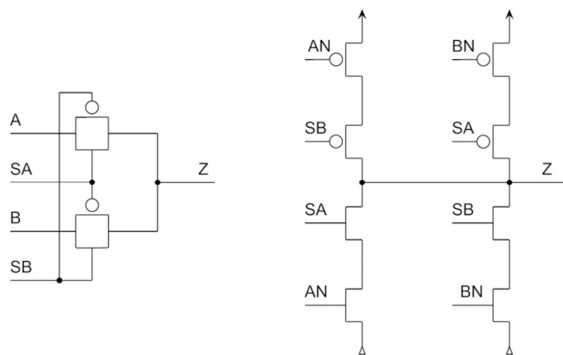

Figure 4. Clocked Inverters Replacing Cross-coupled Transmission Gates

Output Buffer Design

The output buffer consists of the output transistors, their drivers, input buffers, and programmable resistors. The output transistors are typically made from many transistors in parallel, which allow for the strength to be adjusted for a given customer application. The input buffers are also programmable, allowing for choices between TTL and CMOS levels and the optional inclusion of Schmitt triggers.

The biggest issue in I/O buffer design in SOI is the ESD protection. In traditional silicon I/O buffers, the parasitic diodes on the drains serve as an essential component for ESD protection. Their relatively large size provides the current carrying capability needed to survive an ESD event.

With SOI, there are no substrate diodes. The only diode available is the parasitic bipolar device between the drain and the substrate. It was used for ESD protection. Overall, the foundry recommendations for ESD structures were followed.

Figure 5 shows the I/O buffer layout, with the bond pad, the output transistors and their drivers, the input resistor, the protection diodes, the Schmitt trigger logic, and the programmable pullup and pulldown resistors.

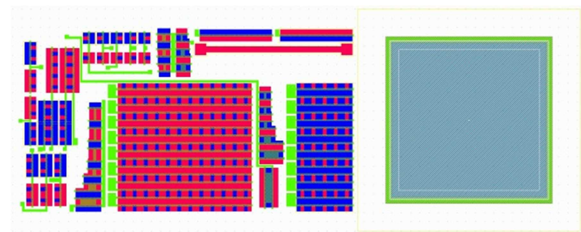

Figure 5. I/O Buffer Layout

Gate Array Design

The design of the gate array is straightforward. An array of gates is surrounded by output buffers. This approach leaves the corners of the chip unused, as the placement of the I/O buffers and power busses prevent easy access to the corners. One corner is needed for the die identification, revision letters and test structures.

Tekmos fills the other three corners with an analog array. The analog array consists of longer L transistors, capacitors, and resistors which can be used to build simple analog circuits when needed (Figure 6). Since the corners lie under the Metal-3 power rings, the analog array must be routed using only Metal-1 and Metal-2. Like most analog circuits, manual routing is required.

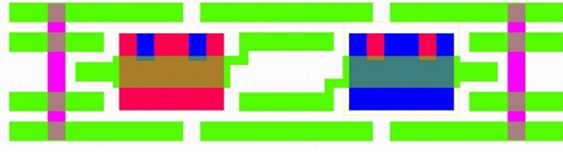

Figure 6. Analog Block

Figure 7 is a die photograph. The metal fill patterns are suppressed in one corner to provide an orientation mark visible to the naked eye that aids in assembly. The circuitry for a specific design appears as a dark area in the center of the chip.

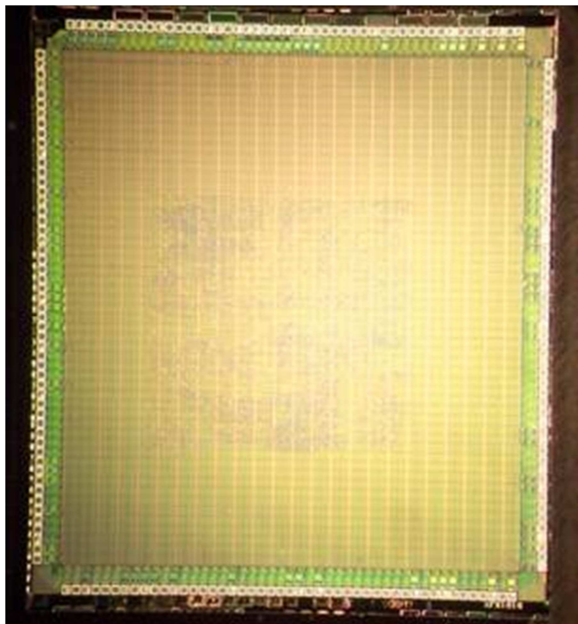

Figure 7. Die Photograph

Electrical Modeling

Delay files for logic components were created using Spice and logic building blocks from an existing digital library. The delay numbers were calculated for the temperature ranges from 0°C to 250°C, over the expected voltage range, and across process variations.

By using the standard digital library and having delay files that represent the high temperature performance, any digital design can be mapped into a high temperature ASIC.

Implementation in an FPGA Conversion

The customer design chosen was in an Actel (now Microsemi) A42MX09 FPGA. The design was converted into the standard Tekmos library, and simulated. While the design was functional, simulation showed it would not reliably work at the required 10MHz. This speed issue was caused not only by the 250°C operation but also because the SOI process was intended for 5 volt operation and this implementation used a 3.3 volt supply.

Conversions from FPGAs to gate arrays often require pushing the speed performance of customer designs, and there are digital techniques for doing so. In this case the design was modified to achieve the required performance and to enhance the fault coverage. These sorts of modifications occur frequently on FPGA conversions and were not considered to be solely related to the temperature requirements.

This part had to fit the pinout of an existing hybrid module. This was not a problem since the Tekmos gate array architecture allows any pad site to be an input, an output or a supply connection.

When the design passed simulations, it was routed, loading violations were fixed, post-route simulations were run, and it was released to manufacturing.

Bonding Choices

A key reliability issue in high temperature operation is open wire bonds caused by the formation of intermetallic compounds at the bonding pad. There was concern that the act of probing the part would introduce topological distortions that might contribute to bond problems. This was resolved by use of two pads on each pin (Figure 8). The circuit can be probed using one pad and still have an un-probed pad for high reliability bonding.

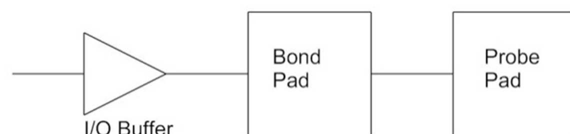

Figure 8. Bond Pad and Probe Pad

Fabrication Choices

The fabrication was made on X-Fab's 1.0µ SOI process. The all tungsten interconnect was chosen for higher reliability. In this process, the bond pads are covered with aluminum to facilitate bonding. The option of depositing a layer of gold on the bond pads after fabrication was not chosen, based on the customer requirements.

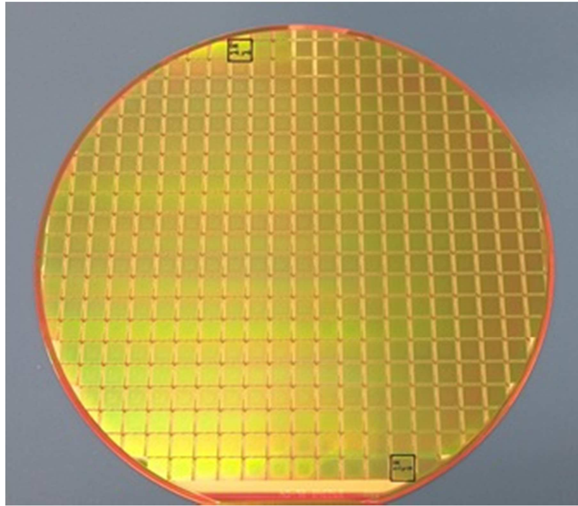

Figure 9. Completed Wafer

Probing and Testing

Wafer probe would have been waived if the parts were to be packaged. However, this application called for probed die to be used in hybrid modules.

The die were probed at 150°C rather than 250°C, primarily due to temperature restrictions on the available probe equipment. Even so, it was necessary to create a special high-temperature probe card for the probing.

Operation

The customer reported that the circuit operated correctly in their application at 250°C and at 305°C. They also reported correct operation for over 1000 hours of operation at 280°C.

Reliability Monitor

Tekmos used its ability to merge designs to include a reliability monitor with the customer design. This consists of a number of ring oscillators designed to measure threshold shifts due to contamination and hot electron injection. The data from this experiment is not yet available.

Conclusions

Tekmos has demonstrated the ability to develop a 250°C ASIC technology capable of implementing arbitrary digital designs.

There are two notable changes to be made in future implementations. The choice of the "Y" grid was expected to generate 10-20 DRC errors per chip, which could easily be corrected. In fact, it generated well over 1000 DRC errors, whose correction introduced delays into the design cycle. The choice of a transistor width of 12µ resulted in the need to buffer an excessive number of signals because of routing delays. The transistors should have been wider.

Acknowledgements

The author would like to thank our customer for sharing the results of their life testing and maximum operating temperature study with us. Additional thanks are due to James Betts, who performed the parameter extraction from the spice models, to Richard Stallkamp who assisted with the preparation of the paper, and to John Hoenig, who did the actual FPGA conversion and made the circuit modifications necessary to achieve the frequency performance at 250°C.

References

[1] B. Ohme; T. Lucking; G. Gardner; E. Vogt; J. Tang; "High Temperature 0.8 Micron 5V SOI CMOS for Analog / Mixed Signal Applications" Proceedings of the 2004 IMAPS International Conference and Exhibition on High Temperature Electronics

[2] www.xfab.com