The Design and Characterization of an 8-bit ADC for 250°C Operation

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Abstract

Many high temperature applications require the measurement of analog voltages. This usually requires the integration of an ADC into the design. While the temperature degradation in performance of digital circuits is well known, the effects of temperature on analog circuitry are much harder to predict. Analog design is often an iterative process in which the characterization knowledge of a fabricated design is used to improve the next iteration of the design. This paper presents the results of the most recent iteration.

This paper describes how the design of an existing 8-bit ADC was optimized for the SOI process. It also presents the characterization of the ADC at various temperatures up to 250°C and shows the effects of increased leakage on the ADC parameters of linearity, accuracy, and conversion speed.

The ADC discussed is a successive approximation design which uses a resistive DAC. The design was modified to take advantage of the resistive characteristics inherent in the SOI process. Specifically, the DAC resistors were formed using N-type diffusion because of their superior matching as compared to using poly. The analog circuitry in the DAC switching and in the comparator required carefully choosing where to use "A" type versus "H" type transistor geometries to prevent inadvertent SCR failures. The ADC design also included a serial interface circuit that facilitates measurements within an oven by minimizing the number of connections required for operation.

The measurements were taken using a 12-bit DAC to generate the analog input voltages to the 8-bit ADC under test. The ADC digital output was compared to the digital input to the DAC. All 4096 measurement points were taken at each voltage and temperature step. The results of these measurements were post-processed to extract the characterization data.

There is a discussion of the results, the effects of leakage on those results, and how these effects might be overcome to produce more accurate ADC circuits in the future.

Key Words: 8-bit ADC, High Temperature Analog, High Temperature ADC

Background

Tekmos designed an 8-bit ADC for inclusion in a customer's ASIC. We included a test mode in the ASIC that allowed the ADC to be operated entirely through external signals. We also included a parallel to serial converter for the data lines to minimize the number of wires that had to be run into the ovens. Using this test mode, the device was bonded into a ceramic package for characterization.

The ADC Design

The ADC is a successive-approximation design using a resistive DAC. The original design was implemented in a 0.6u design for use in the Tekmos 68HC05 and 68HC11 families of microcontrollers.

As shown in Figure 1, the ADC consists of three components: a digital successive approximation register (SAR), which drives an 8-bit DAC, whose output voltage is compared with the external signal by the comparator, which controls the SAR. The SAR also contains a small state machine that accepts the start signal, controls the comparator, and generates the End of Conversion (EOC) signals.

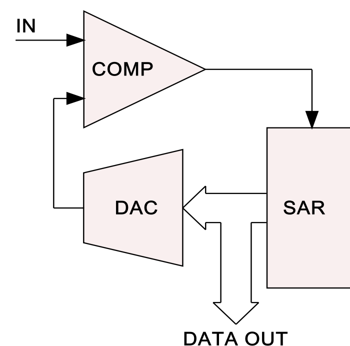


Figure 1 – ADC Design

The 8-bit DAC Design

The resistive DAC consists of a primary string of sixteen resistors. Transmission gates are used to connect a secondary string of 16 resistors to be in parallel with one of the primary resistors. A second set of transmission gates selects one of the secondary resistors to be connected to the comparator.

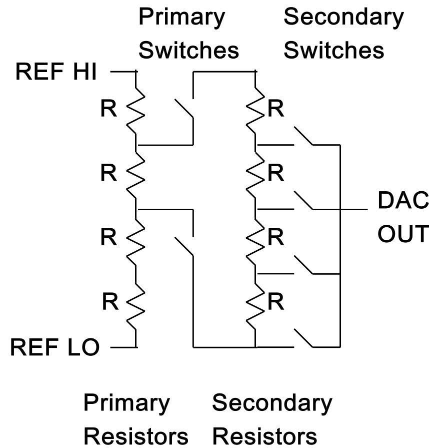


Figure 2 – DAC Design

Figure 2 shows the DAC design. The figure is simplified by using 4-long resistor strings instead of 16-long resistor strings. As long as the resistive value of the secondary string is large with respect to the unit resistors of the first string, then the loading effects of putting the resistors in parallel is negligible.

Our original design used poly resistors for the DAC. Bulk silicon processes use poly resistors because the voltage coefficient is virtually zero. This near zero voltage coefficient outweighs the fact that poly resistors have a much worse matching coefficient than P and N diffusion resistors. Also, the parasitic capacitance that affects DAC speed is significantly less with poly resistors than with diffused resistors.

In the SOI process, a diffusion resistor does not have any junctions. And without a junction, the voltage coefficient approaches zero. This lack of a junction also reduces the stray capacitance. These effects make diffused resistors a better choice than poly resistors for the SOI process.

We used N diffusion resistors in the DAC since they had better matching than P resistors. We anticipated that their better matching characteristics would help compensate for increased leakages encountered at high temperatures.

We were concerned because we had not previously encountered matching N+ resistors in a DAC. Discussions with our fab engineers assured us that there was not some other effect that we were overlooking. They concurred with our choice.

Resistor matching was enhanced by the use of dummy resistors surrounding the resistor strings to prevent etching edge effects. The layout of the resistor ends were designed so that contact misalignment would cancel out and not affect the resistor matching.

Another issue was the design of the transmission gates that are used to connect the resistor strings. The SOI process allows for two transistor layout types, known as “A” and “H”. The “H” architecture was used because it allows for reversal of source and drain, necessary in transmission gates when logic levels reverse. Since the “H” transistors are weak, many were paralleled to achieve the strengths required to switch the resistors in the allotted time. The tradeoff is that the increased transistor area increases the leakages which will affect accuracy.

The Comparator Design

The comparator consists of a string of inverters. The inverters are kept in a balanced condition with the outputs shorted to the inputs. The external voltage is sampled on a capacitor before the measurement begins. The DAC voltage is also capacitively coupled to the inverter inputs, causing the inverter string to switch high if the DAC has a greater voltage and to switch low if the DAC has a lower voltage. The comparator design is shown in Figure 3.

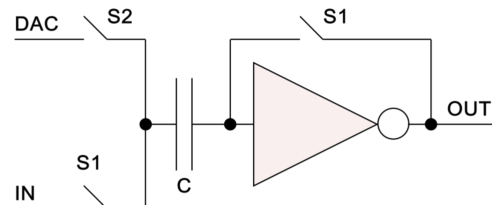


Figure 3 – Comparator Design

During the sample time, the S1 switches are closed and the S2 switch is open. The capacitor is

charged with a voltage equal to the input voltage minus the inverter switching threshold.

During the ADC operation, the S1 switches are opened, and switch S2 is closed and connected to the DAC. If the DAC voltage is greater than the input voltage, then the inverter will switch low. And if the DAC voltage is less than the input voltage, then the inverter will switch high.

One possible failure mechanism is that the voltage on the capacitor will be affected by transistor leakage, and that will cause measurement errors.

Additionally, the poly0 to poly1 capacitors used with the bulk silicon process are not available in the SOI process. Capacitors were made of four layer stacks: poly1, metal-1, metal-2, and metal-3 with alternate layers connected. The capacitance per unit area of this stack is lower than the poly0 to poly1 capacitors in the bulk process, resulting in a significant area penalty.

The Physical Layout

Figure 4 shows the ADC layout. The area of the ADC is 0.5 mm^2. The SAR is the two vertical columns on the right. The SAR was implemented as gate array logic.

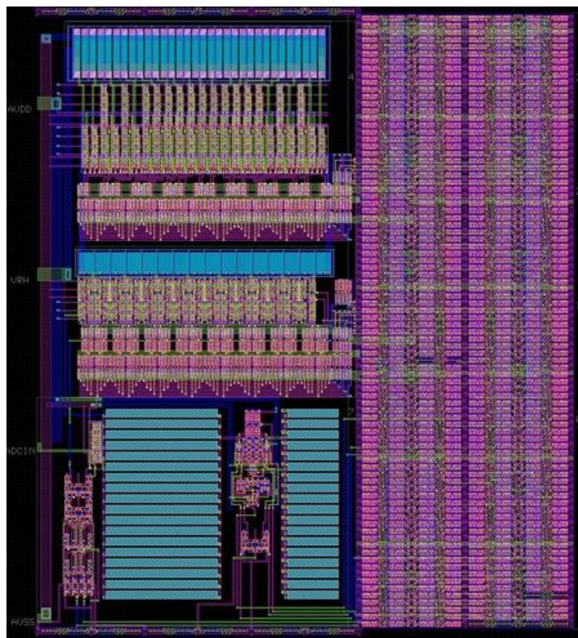


Figure 4 – ADC Layout

The DAC is made from the two horizontal structures on the upper left side. Each structure is one of the resistor strings and their associated switches and switch drive logic.

The comparator is at the lower right. The blue pars are capacitors, with the main coupling capacitor being on the left.

Test Mode Circuitry

The ADC is passive, requiring a clock and a start signal to perform a conversion. An EOC (End-Of-Conversion) signal marks the end of the conversion. It is meant to be controlled.

Since our test mode disconnected the ADC from the ASIC, we had to design a controller that would generate the start signal and the clock. We also needed to read the data bits after the conversion and shift them out serially in order to minimize the number of wires required to exercise it at temperature.

Test Setup

We used a production tester, a Griffin III from Hi-Level, to generate and record all digital signals. The tester also provided the inputs to an AD8522 dual, 12-bit DAC. One DAC was used to provide the analog input and the other DAC provided the reference voltage. Having a single monolithic analog source both improved the accuracy and simplified the measurements. See Figure 5.

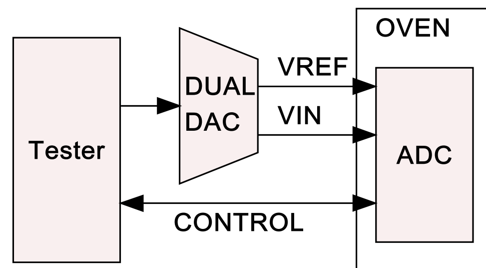


Figure 5 – Test Setup

External 12-bit DAC

Our initial plan was to use a voltage reference of 5.12 volts, which would have made each ADC step 20 mV. However, during the design of our test card, we realized that it would be simpler to use a 5 volt DAC with a 4.096 volt full scale output. This makes the theoretical ADC step 16 mV, and gives us the ability to determine the true step value to 1 mV.

Figure 6 - Board in oven

Test Board

The test PC board was made from polyimide material that is rated up to 280ºC. The material allows for brief excursions to higher temperatures. We went slightly beyond that point. The purpose of the board was to provide a means to connect the wires to the part.

The solder had a melting point of 300ºC. Again, we made brief excursions to higher temperatures.

The board was also constrained to a 600 mil width to allow it to fit through a small portal at the side of the oven. The board also contained a strain relief for the wires, since it was mechanically supported in the air by the wires. See Figure 6.

Wiring

We were using wires with a 450ºC insulation rating. While these are fine for digital signals, we were concerned about the three analog signals. Ideally, we would use coax, but none with a high temperature rating was available at the time testing was done. Instead of coax, we used two additional wires that were twisted around the analog wires to provide shielding.

Oven

The oven was a Blue M oven rated at 350ºC.

Experimental Procedure

After initializing the reference DAC, the tester goes into a cycle of programming the analog input DAC, triggering an ADC measurement, and then recording the ADC output. This was repeated for all 4096 codes. The tester log showing the measurement results was stored for subsequent processing. Then the temperature was incremented and the procedure repeated. We started at 20ºC, and performed measurements up to 320ºC.

Experimental Results

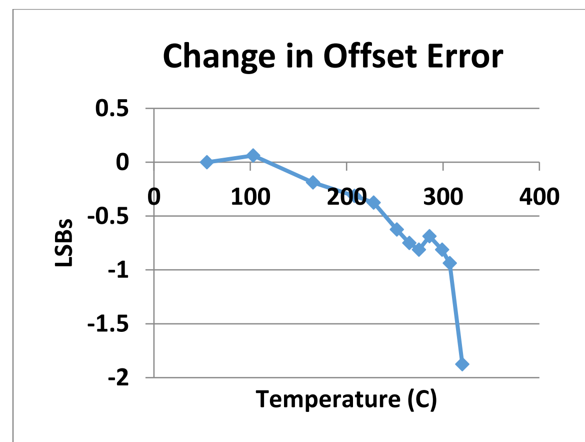
The ADC worked over the entire temperature range, though there was degradation of performance above 275ºC. We ran additional measurements up to 320ºC because the parameter shifts gave insight as to the performance of internal analog nodes.

The data was normalized to the 50ºC results. Our 20ºC data was measured with the oven off, and there was a noticeable difference in results after the oven had been turned on. Because of this difference, we chose to normalize the data to 50ºC.

Offset Error

The offset error, also known as a zero error, is the voltage difference between when the ADC switches from 00 to 01, and ½ LSB.

Graph 1 shows the change in offset error over temperature.



Graph 1 – Offset Error

The offset error shifted by 0.625 LSB at 250ºC, 0.81 LSBs at 300ºC, and 1.8 LSBs at 320ºC.

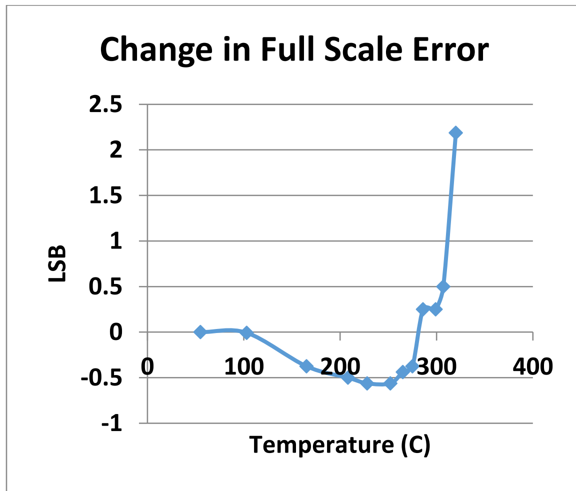
We believe that the change in offset was due to leakages affecting the sample and hold capacitor.

In the design, the negative voltage reference was internally connected to the analog VSS signal. While not ideal for measurements, this was required by the application. As a result, the ground current introduces a slight error in this measurement. This can be compensated for by using the offset error as an adjustment when analyzing subsequent measurements.

Full Scale Error

The full scale error, also known as a gain error, is the voltage difference between when the ADC switches from FE to FF and the full scale voltage – ½ LSB.

Graph 2 shows the change in full scale error over temperature.



Graph 2 – Full Scale Error

The full scale error had shifted by -0.56 LSBs at 250ºC. The direction changed at 273ºC, and reached a positive 2.19 LSB by 320ºC.

In the design, the positive voltage reference is internally connected to the analog VDD signal. As with the offset error, this introduces a small error in the full scale error measurement.

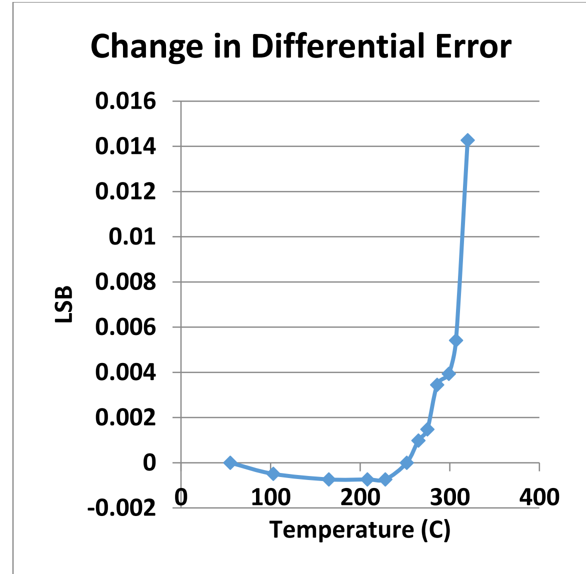
Differential Non-Linearity

The differential non-linearity is a measure of the width of each step, and normalized to the width of a step of an idealized ADC.

Graph 3 shows the change in the average differential non-linearity with temperature. The change was 0 LSB at 250ºC, and reached 0.014 LSB at 320ºC. The increases in leakage current compensated for what was a negative trend at lower temperatures.

Integral Non-Linearity

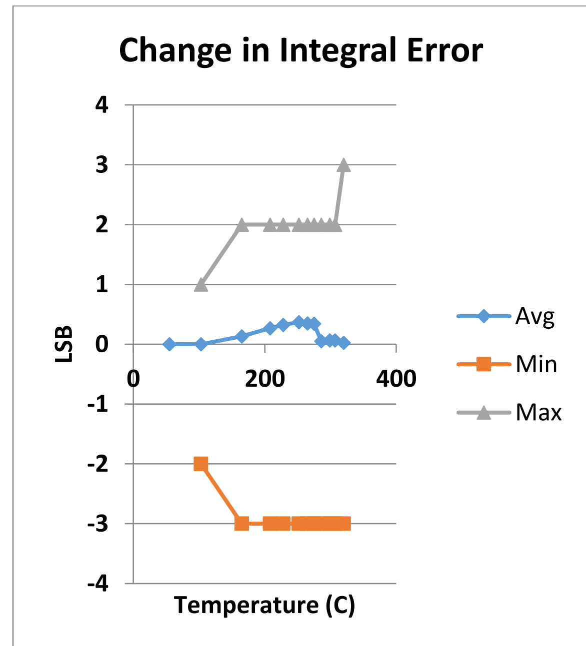
The integral non-linearity shows how far off the device is from an ideal ADC. It may be considered as the sum of the differential nonlinearities.



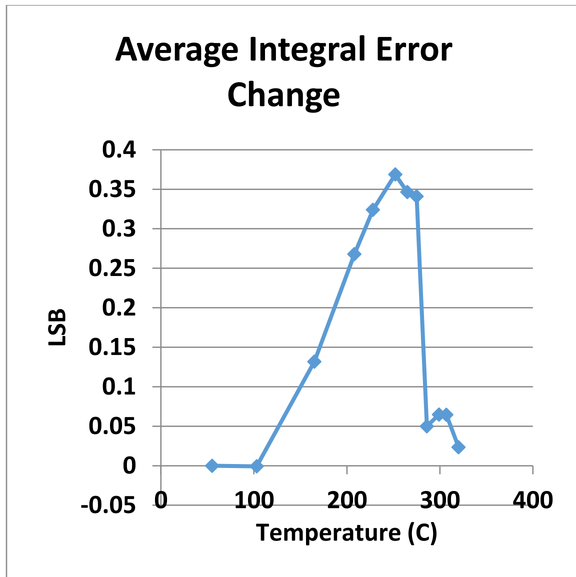
Graph 3 – Average Differential Nonlinearity.

Integral Error

The integral error is presented and both the maximum and minimum errors as well as the average error. (Graph 4) The extremes are likely driven by noise in the oven. The average error rose slightly with temperature, reaching a peak of about 0.36 at 250ºC before declining at the higher temperatures. The changes in the average error are detailed in Graph 5.



Graph 4 – Integral Error



Graph 5 – Average Integral Error Change

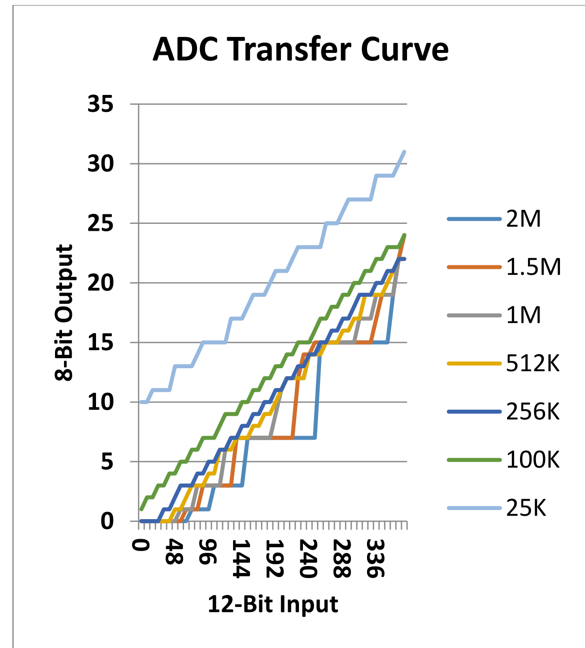
Leakage in the Sample and Hold Capacitor

After observing the changes in parameters at above 273ºC, we suspected that this was caused by leakage which drained off the charge contained in the sample and hold capacitor.

In order to confirm this, we ran another experiment at 286ºC in which we varied the clock frequency of the ADC. The ADC has a maximum and a minimum frequency. The maximum frequency is set by the response time of the DAC. The DAC needs time to settle to the specified voltage. If the clock is running too fast, the DAC will have an incorrect voltage on it, and the ADC will make an error. This shows up as missing codes.

If the frequency is too slow, junction leakages can change the sampled input voltage, resulting in an incorrect reading.

Graph 6 shows the ADC transfer curve for various clock frequencies, ranging from 25 KHz to 2 MHz. The overall accuracy is quite bad at lower frequencies. At the same time, the device does not work correctly with frequencies of 1 MHz or above. Above 275ºC, the upper and lower limits meet, and the accuracy begins to fall off. This graph shows a detail of the ADC transfer curve. The measurements were taken at 286ºC. In this graph, we can see that the transfer curve is shifting for clock frequencies of less than 250ºC. The slower clock frequencies provide more time for the charge to leak off of the sample and hold capacitor.



Graph 6 – ADC Operation at Various Frequencies

The graph also shows that for clock frequencies of 1M and higher, the DAC cannot switch fast enough, and the ADC is starting to skip codes.

The large degradation in performance above 300ºC is likely a result of a convergence of the minimum and maximum clock speeds.

Conclusions

The ADC worked well up to 250ºC. Beyond that point, the leakages affected the capacitor used to sample and hold the input voltage. The loss of charge on that capacitor affected the performance.

This can be addressed by increasing the size of the sample and hold capacitor, and decreasing the physical size of the switches. The smaller switches can be compensated for by increasing the specified sample time.

The DAC appeared to be operating correctly up to 320ºC. It appears that the high temperature leakage is not affecting the DAC.

The digital logic in the SAR performed correctly at 320ºC and with a 2M clock frequency.

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