

Features

- Exact replacement of existing FPGAs, including Xilinx, Altera, Actel, Lattice and many others
- Identical package footprint means no board redesign
- Emulation of initialization sequence
- Emulation of JTAG circuit
- 0.35u Technology for older FPGAs
- 0.18u Technology for newer FPGAs
- Easy engineering interface. We work from your existing files.
- Design recreation from programming files on some devices
- Flexible supply pin placement
- Automatic Test Program Generation (ATPG)
- Small or large production quantities supported

Major Customer Benefits

- Save 50% or more on cost of FPGAs / CPLDs
- Solve product obsolescence issues
- Guaranteed to work – no risk
- Fast turnaround on most FPGA replacements

FPGA Conversions

FPGA conversions consist of reimplementing an FPGA design into an ASIC. There are a number of reasons to convert a design. An ASIC will have lower unit cost, lower power, higher performance, and more package flexibility. These benefits have to be weighed against the NRE charges, and the lack of reprogrammability.

Tekmos provides customers with comprehensive engineering support. We accept designs on an "as is" basis, translate them into our internal cell libraries, and perform the engineering work necessary for a successful conversion.

FPGA Conversion Flow

Tekmos accepts designs in any format. Most designs arrive as FPGA netlists. We also convert ASIC netlists that have been implemented in another vendor's library.

FPGA Conversion

We request that the customer provide us with the original design files, along with any simulations that may exist. We can accept either pre-synthesis RTL level designs, or gate level designs.

In cases where the validity of the design files is in question, Tekmos can verify the design by comparing the simulated performance against actual results derived from the FPGA.

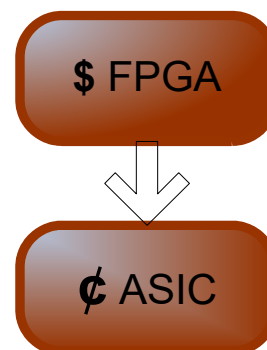
Simulations and Sign-Off

Original simulations (if they exist) will be enhanced with Tekmos generated simulations and used for production testing.

Replacing an FPGA or existing ASIC means that Tekmos is responsible for the post-route signoff. Customer participation, while optional, is encouraged.

Prototypes

The design will be fabricated, assembled, and tested. Prototypes are available in about 10 weeks after tape-out.



Quotations

Within a given FPGA type, the size of the individual FPGA design can vary considerably, depending on the number of gates, the amount of memory, and the number of used pins. On the other hand, the cost of the ASIC replacement is directly linked to the design size. The design netlist must be reviewed to provide an exact quotation.

Tekmos can provide a budgetary quotation based on the full FPGA part number and desired annual volume. A more accurate budgetary quotation can be obtained if the FPGA utilization report is provided.

Simulations

Simulations become increasingly important for the larger FPGA devices. We use functional simulations to verify that the conversion process has not introduced race conditions into the design. They provide a level of verification that is not available through static timing analysis.

If simulations are not available, then we will have to create them. Depending on the size and nature of the circuit, there may be additional charges to create simulations.

Embedded Cores

Some FPGAs come with embedded cores, such as Power PCs. If your design uses embedded cores, and you do not own the rights to that core, then we cannot convert the design into an ASIC.

FPGA Families

Suitability for Conversions

Most, but not all FPGA are candidates for ASIC conversion. Designs vary widely in size, memory content, power supply requirements, and speed. Each design must be evaluated individually. The following tables show the different FPGA families and the general suitability for conversion.

T Technology / Power Supplies

In general, the gate array fabrication technology sets the core power supply. Any given gate array can be logically replaced by an ASIC using an older technology. However, using a lower voltage supply degrades the ASIC performance. This can be compensated for by either running the ASIC from the I/O supply, or by changing the core supply.

P Pin Count

Some FPGAs have very high pin count. Increased pin count increases costs exponentially, and may make a conversion uneconomical. The use of more than 200 (0.35u) or 250 (0.18u) pins will affect the NREs and unit pricing.

R RAM size

FPGAs contain varying amounts of RAM. The use of large amounts of RAM can exceed the internal RAM in a given ASIC. This will require the selection of a larger ASIC, increasing the cost.

S Speed

Many FPGAs support very fast output timing, which can be difficult to achieve in an ASIC using an older technology. These timings are not always required in a customer's application, and are frequently waived. In general, the minimum timings for 0.35u ASICs are about 7 ns and for 0.18u ASICs are about 5 ns.

T No problem with conversion.

T May be issues with some FPGA characteristics.

T Some FPGA features are not available.

Xilinx Virtex Series

Tekmos Technology	0.18u				0.35u			
	T	P	R	S	T	P	R	S
Virtex 5								
Virtex 4								
Virtex II Pro								
Virtex II X								
Virtex II								
Virtex EM								
Virtex E								
Virtex								

Xilinx Cool Runner Series

Tekmos Technology	0.18u				0.35u			
	T	P	R	S	T	P	R	S
CoolRunner II								
CR XPLA3								

Altera CPLDs

Tekmos Technology	0.18u				0.35u			
	T	P	R	S	T	P	R	S
MAX II								
MAX 3000A								
MAX 7000								

Xilinx Spartan Series

Tekmos Technology	0.18u				0.35u			
	T	P	R	S	T	P	R	S
Spartan 3								
Spartan 3E								
Spartan 3L								
Spartan IIE								
Spartan II								
Spartan XL								
Spartan								

Altera FPGAs

Tekmos Technology	0.18u				0.35u			
	T	P	R	S	T	P	R	S
Cyclone II								
Cyclone								
Stratix II								
Stratix								
Stratix II GX								
Stratix GX								

Xilinx Mature Series

Tekmos Technology	0.18u				0.35u			
	T	P	R	S	T	P	R	S
XC9500XL								
XC9500XV								
XC9500								
XC5200								
XC4000								
XC3000								

Altera Mature CPLDs

Tekmos Technology	0.18u				0.35u			
	T	P	R	S	T	P	R	S
MAX 7000B								
MAX 7000S								
MAX 9000								
Classic								

Altera Mature FPGAs

Tekmos Technology	0.18u				0.35u			
	T	P	R	S	T	P	R	S
ACEX 1K	Green	Yellow	Green	Green	Yellow	Yellow	Green	Purple
APEX II	Green	Yellow	Yellow	Yellow	Purple	Yellow	Purple	Purple
APEX 20KC	Green	Yellow	Green	Yellow	Purple	Yellow	Yellow	Purple
APEX 20KE	Green	Yellow	Green	Green	Yellow	Yellow	Yellow	Purple
APEX 20K	Green	Yellow	Green	Green	Green	Yellow	Yellow	Yellow
FLEX 10KE	Green	Yellow	Green	Green	Green	Yellow	Yellow	Yellow
FLEX 10KA	Yellow	Yellow	Green	Green	Green	Yellow	Yellow	Green
FLEX 10K	Yellow	Green	Green	Green	Green	Yellow	Yellow	Green
FLEX 6000/A	Yellow	Green	Green	Green	Green	Green	Green	Green
FLEX 8000	Yellow	Green	Green	Green	Green	Green	Green	Green

Actel Antifuse

Tekmos Technology	0.18u				0.35u			
	T	P	R	S	T	P	R	S
Accelerator	Green	Yellow	Green	Green	Yellow	Yellow	Yellow	Yellow
SX-A	Yellow	Yellow	Green	Green	Green	Yellow	Green	Green
SX	Yellow	Green	Green	Green	Green	Yellow	Green	Green
eX	Yellow	Green	Green	Green	Green	Green	Green	Green
MX	Yellow	Green	Green	Green	Green	Green	Green	Green

Actel Legacy

Tekmos Technology	0.18u				0.35u			
	T	P	R	S	T	P	R	S
3200DX	Yellow	Green	Green	Green	Green	Green	Green	Green
1200XL	Yellow	Green	Green	Green	Green	Green	Green	Green
ACT3	Yellow	Green	Green	Green	Green	Green	Green	Green
ACT2	Yellow	Green	Green	Green	Green	Green	Green	Green
ACT1	Yellow	Green	Green	Green	Green	Green	Green	Green

Altera Mature Others

Tekmos Technology	0.18u				0.35u			
	T	P	R	S	T	P	R	S
Mercury	Yellow	Yellow	Green	Yellow	Purple	Yellow	Yellow	Purple
Excalibur	Green	Purple	Green	Yellow	Yellow	Purple	Purple	Yellow

Actel Flash

Tekmos Technology	0.18u				0.35u			
	T	P	R	S	T	P	R	S
M7 Fusion	Yellow	Yellow	Green	Green	Purple	Yellow	Purple	Purple
Fusion	Yellow	Yellow	Green	Green	Purple	Yellow	Purple	Purple
M7 ProASIC3	Green	Yellow	Green	Green	Purple	Yellow	Purple	Purple
ProASIC 3	Green	Yellow	Green	Green	Purple	Yellow	Purple	Purple
ProASIC Plus	Green	Yellow	Green	Yellow	Yellow	Yellow	Yellow	Yellow
ProASIC	Green	Yellow	Green	Yellow	Yellow	Yellow	Green	Yellow

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Revision History

Date	Revision	Description
5/26/06	1.0	Initial release
3/10/11	1.1	Update, include more on 0.18u, test issues
11/25/14	1.2	Clarifications and Fix typographical errors

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