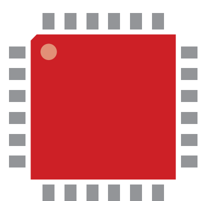
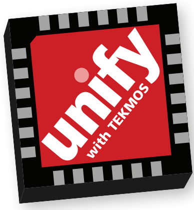
Unify ASICs
for your System in a Package



TEKMOS

Introducing Unify ASICs



Applications for System in a Package are driven by the requirements of space, power, and development time. The total solution needs to be small. It typically runs off of a battery. And it needs a quick time-to-market.

The major semiconductor suppliers have developed a number of cost effective blocks that can meet 90% of the requirements of an application. It is the last 10% that is the problem.

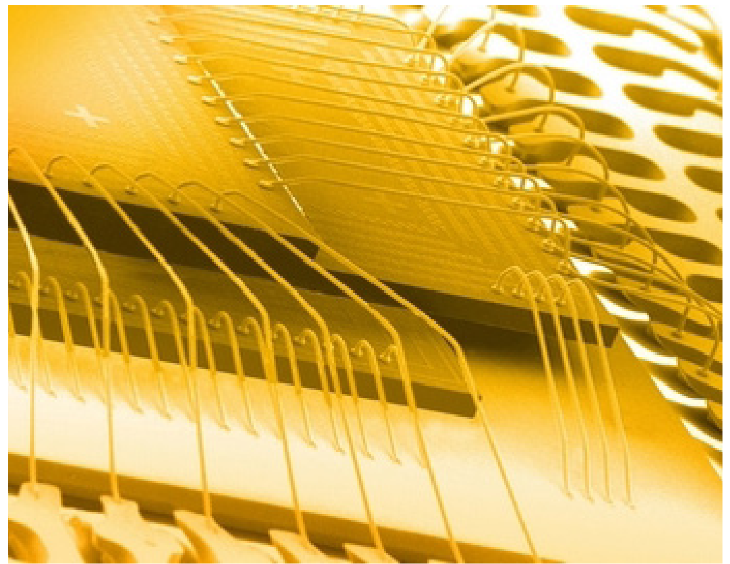
Developers typically face two approaches for the last 10%. You can build what you need out of discrete components. This is inexpensive, but requires a lot of board space. Or you can take a SOC (System on a Chip) approach. This will work, but can be very expensive, since the presence of wireless interfaces and ARM processors requires advanced processing to accommodate the diverse requirements of diverse technologies as well as expensive NREs. And such solutions require more development time because of the chip complexity.

Tekmos has a third approach. We create a cost effective ASIC using an appropriate technology to implement the missing 10%. Then we use stacked die assembly technology to add the processor, wireless communications, sensors, and other standard features. This results in a single chip implementation of your system, bringing you all of the advantages of an ASIC, but without the high NRE charges. Our name for this program of combining standard building blocks with your unique IP is Unify.

Stacked Die Assembly

The key to mixing fab technologies is stacked die assembly. This involves stacking different die in a single package, and then bonding each chip to each other or to the outside world. This is how Tekmos combines a microcontroller, RF communications, and an ASIC into a single package. Stacked die technology is not new. Tekmos has been using it for more than 15 years as a method of integrating flash memory into our microcontroller and memory designs. The ASIC also serves as a means of interconnect for the system components. This resolves the issue of incompatible pinouts between the stacked components.

Die can be stacked in any package. In the larger

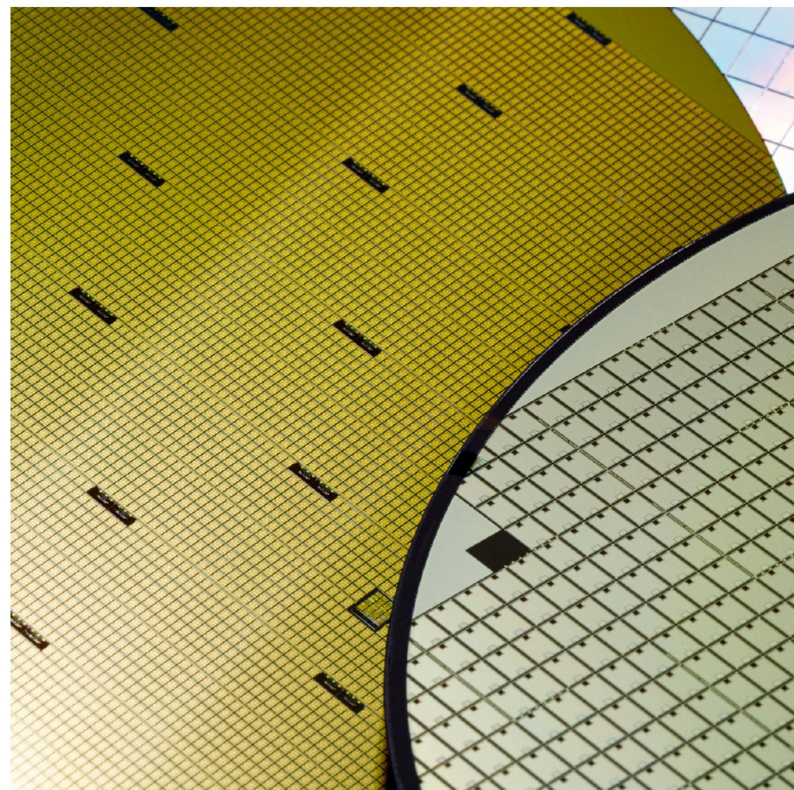


Picture of Stacked Die.

BGA packages, die can be stacked side by side as well as on top of each other. And in some cases, we can also include components that we cannot put on the ASIC such as large capacitors, and crystals. No matter what package we use, the customer wins by having a single, highly integrated device for their system.

Technology

It is a fact that the NRE costs roughly double for each generation of fab technology. What is not so well understood is that the newest technology may not be required for all portions of the design. The stacked die approach of Unify ASICs allows



Tekmos to mix technologies, and use the most cost effective solution for each die in the stack. Thus the processor can be made in a 45 nm technology, while the ASIC itself can be made in a 180 nm technology. The key to a cost effective SiP solution is to just use the technology you need, but no more.

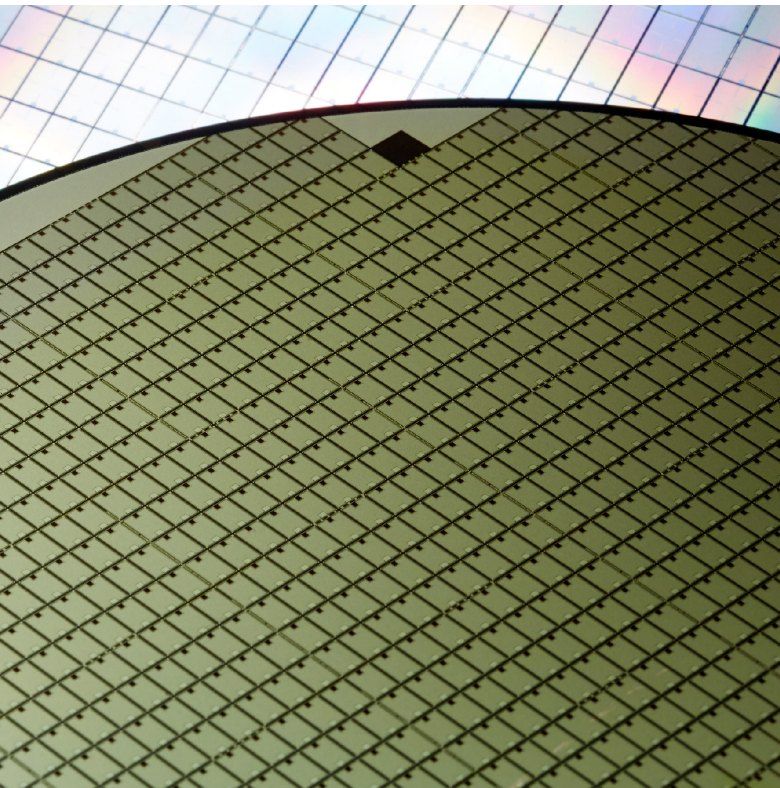
Mixed Signal ASICs

A Unify ASIC from Tekmos can include mixed signal circuitry. We can add the interface your design needs, to connect with the outside world. This can be sensor integration, additional power supplies, battery management, or signal conditioning.

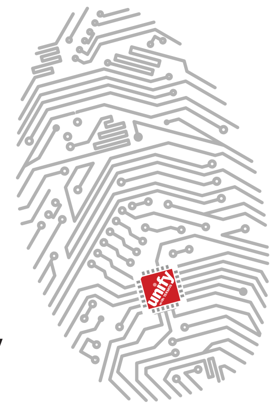
Starting from a rich library of op-amps, voltage references, filters, charge pumps, and switches, we can provide the mixed solution that you need to succeed in your market.

Cost of ASICs

There are many stories of companies spending $20M or more to make an ASIC. And some of these stories are true. But an ASIC does not have to be expensive. The Tekmos approach of unifying existing parts with a technology appropriate ASIC in a stacked die package will reduce the cost substantially. Our graduated approach to NREs allows the initial parts to be made with engineering lots or shuttle runs, which reduces the initial investment, and allows initial production without high volume commitments.



Design Security



There are two types of security issues with embedded systems. The first involves hacker attacks, and these are typically dealt with by the processor. The other security issue is the security of the design itself. Any product made out of standard parts can be easily copied. But if the design includes a proprietary ASIC, then it becomes much more difficult to copy. And by working with Tekmos, the designer can be certain no one else has access to his design or to his Unify ASICs without his permission.

Engineering Resources

Chip design requires a lot of specialized knowledge, and access to a lot of expensive tools. That is the job of Tekmos. The customer only needs to define their system in RTL, and to have verified their design in a prototype, which is usually an FPGA. We will do the rest. We will need some access to the system designer, and to have the customer participate in periodic design reviews.

Ramping Up Production

With a new product development, it is common for the design to change, particularly after the product has had its first exposure to customers. What sounds great in a marketing meeting may need adjustments to achieve customer acceptance. This is why Tekmos offers the ability to run engineering lots or shuttle runs on the initial silicon. This is a great way to produce 100s or 1000s of parts without a large investment in photomasks. Then, when the product has reached market acceptance, we can invest in a full mask set to support high volume and lowest cost.

Contact us and learn how a Unify ASIC from Tekmos can launch your product into the marketplace.

Automotive, Medical, Military, and Industrial

512-342-9871 phone
Sales@Tekmos.com
www.Tekmos.com