Unify System in a Package For The Internet of Things

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Unify SiPs

Applications in the internet of things are driven by the requirements of space, power, and development time. The total solution needs to be small. It typically runs off of a battery. And it needs a quick time-to-market.

The major semiconductor suppliers have developed a number of cost effective blocks that can meet 90% of the requirements of an application. It is the last 10% that is the problem.

Developers typically face two approaches for the last 10%. You can build what you need out of discrete components. This is inexpensive, but requires a lot of board space. Or you can take a SOC (System on a Chip) approach. This will work, but can be every expensive, since the presence of wireless interfaces and ARM processors requires advanced processing to accommodate the diverse requirements of diverse technologies as well as expensive NREs. And such solutions require more development time because of the chip complexity.

Tekmos has a third approach. We create a cost effective ASIC using an appropriate technology to implement the missing 10%. Then we use stacked die assembly technology to add the processor, wireless communications, sensors, and other standard features. This results in a System in a Package (SiP) implementation of your system, bringing you all of the advantages of an ASIC, but without the high NRE charges. Our name for this program of combining standard building blocks with your unique IP into a SiP is **Unify**.

Creating a Unify SiP

A Unify SiP starts with the customer defining what they want to include in the system. This is a combination of standard products, and functions that can be included in the ASIC portion. Tekmos engineering works with the customer to evaluate choices, evaluate the standard products, and defining the package and pinout.

When appropriate, Tekmos will construct a PCB based prototype of the final Unify SiP. This can be used to verify the design and to assist with the system software development.

The workflow then divided into parallel paths. One path is the typical ASIC design and fabrication flow. Another path covers the acquisition of the standard products used in the SiP. A third path covers package design issues. Sometimes, a unique BGA substrate or QFN leadframe will need to be designed.

The paths converge at package assembly. The parts are assembled, tested, and the prototypes delivered. Production can begin after prototype approval.

System Definition

A Unify SiP starts with the customer defining what they want to include in the system.

To begin with, a division is made between what is to be incorporated within the ASIC and what circuits are going to be added as stacked die.

Component Considerations

Some components can be included within the ASIC. These components are typically part of a signal path, or a bias generation, and can be implemented as a mixed signal section within the ASIC.

There is a size limitation with the package. Simply put, large components are not going to fit in a small package. This includes inductors that are used in power supplies, and bypass capacitors. Any component that we do use will generally need to be under 0.5 mm in thickness.

Purchased Die Considerations

The first consideration about the other die that we stack with our ASIC is if they are available. Most manufacturers will offer their product in die form. More specifically, we need KGD (Known Good Die) in wafer form.

Why? Because we need to thin the wafers in order to get them to fit in the package. Wafer thinning, also known as back-grinding, cannot be done on loose die.

Most die sales are done for hybrid applications, which typically do not have a height restriction. So a wafer sale may not be part of a manufacturer's flow. Also, the wafer yield information is knowable when you purchase a wafer, and many manufacturers consider that proprietary. This can usually be addressed with an NDA.

Other manufacturers may have products that are not complete until final test. For example, a processors bootstrap code can be downloaded after the probe test. In such cases, Tekmos has the technical expertise to complete the testing.

If a manufacturer's product is not available, then either an alternative part must be found, or that function will have to be excluded from the Unify design.

Pinout Considerations

Small packages have limited pinouts. We can get about 60 pins in a QFN package and up to 100 pins in a BGA package. Higher pin counts require larger packages, and that tends to negate the size advantages obtained through the Unify program.

The pin count can be reduced by either increasing the integration level by adding another chip which is the destination of the wires, or removing the source ship. Fortunately, higher levels of integration tend to reduce the external wire count.

Power Considerations

Fortunately, most Unify applications are low power, since heat dissipation can be a problem in stacked die architectures. This can be addressed by placing the hottest die on the bottom where it can be attached to the package pad, or on the top where it can connect to an external heat sink.

Package Considerations

Die can be stacked in almost any package. However, it might not make economic sense unless the Unify package saves space.

This typically results in either a QFN or a BGA type package. These are usually square, with an integer multiple of millimeters per side. The most common sizes range from a 4x4 mm to a 9 x 9 mm package.

The two constraints on the package size are pin-count and die size. Obviously, the package has to be large enough to hold all of the pins.

The package also needs to be larger than the largest die in the stack by about 1 mm. In most cases, the Unify ASIC is the largest die, since it has to incorporate the bond pads necessary to connect the other die in the package. Each case is different, but the Tekmos ASIC may need to be 0.7mm larger than the next largest die.

Why is the ASIC Required?

A Unify SiP requires a Tekmos ASIC for two main reasons. These are matching the internal pinouts and testability.

Matching Internal Pinouts

There is a lot of package development occurring today with 2.5D and 3D assembly techniques, including TSVs (Though Silicon Vias) and interposers. TVSs require that the die have compatible layouts. A TSV will not work if the hole it cuts is not aligned with the chip beneath it.

Stacking identical memories works with these approaches. But the differing die in a Unify SiP will not have common pinouts and sizes. So we run most wires to the Unify ASIC, and let it resolve the interconnect issues.

Interposers resolve interconnect issues, but do nothing for testability.

Testability

The assembly process breaks 2 to 5 percent of the Unify SiPs, so we must test all parts. This is complicated because many of the internal nodes in the Unify SiP are hidden from the outside world.

The Tekmos ASIC contains all of the BIST (Built In Self Test) logic necessary to fully test the part. The BIST methods and circuitry will depend on the types of components included in the Unify SiP.

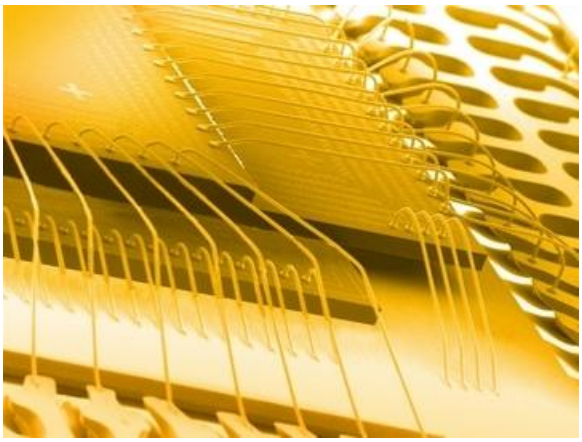
Additional ASIC Benefits

The Tekmos ASIC can also include system functions that are not available in the standard parts. This can be mixed signal functions, or logic functions currently in a FPGA.

In either case, the presence of a Tekmos ASIC provides design security by making your system much more difficult to copy or duplicate.

Stacked Die Assembly

The key to mixing fab technologies is stacked die assembly. This involves stacking different die in a single package, and then bonding each chip to each other or to the outside world. This is how Tekmos combines a microcontroller, RF communications, and an ASIC into a single package. Stacked die technology is not new. Tekmos has been using it for more than 15 years as a method of integrating flash memory into our microcontroller and memory designs. The ASIC also serves as a means of interconnect for the system components. This resolves the issue of incompatible pinouts between the stacked components.



Picture of Stacked Die

It is desirable to minimize the number of internal bond wires within the Unify SiP, as the total number of internal bonds is directly related to the package price. Also, since each bond pad requires about a 50u pitch, too any wires can increase the ASIC size, which both increases the cost and may require a larger package.

One way or reducing the bond wire count is through the use of a flip-chip assembly technique. The standard part with the largest pin count will have an array of solder balls attached to it, allowing it to be "flipped" and attached upside down to the ASIC. Other standard parts can then be stacked on top of the flipped chip.

Die can be stacked in any package. In the larger BGA packages, die can be stacked side by side as well as on top of each other. And in some cases, we can also include components that we cannot put on the ASIC such as large capacitors, and crystals. No matter what package we use, the customer wins by having a single, highly integrated device for their system.

Testing a Unify SiP

A Unify ASIC consists of known good die, stacked and interconnected in a single package. Theoretically, it should work and no further testing should be required. Reality is different.

The act of thinning the wafer, and cutting it apart will damage some die. There are occasional bond problems, such as opens from broken bonds or shorts from touching bond wires swept together during the injection of plastic into the mold. And some of the thinned die will crack due to pressures tin the assembly process. As a result, the assembled parts must be tested.

Normal integrated circuit testing is a rigorous check of as may internal nodes as possible. This is to identify microscopic defects that may result in a short or an open on an individual node. Unify ASIC testing is different. We need to check for assembly defects, and we have to check for performance issues related to all of the chips in the package correctly working together. And we have to do this in an environment in which many bonds and chips have no direct access to the outside world. In order to do this, we include BIST (Built In Self Test) circuitry in the Tekmos ASIC.

Checking for open or shorted bond wires involves doing a test that exercises all bond wires. This can be either a direct stimulation of a wire, or indirect confirmation through the usage of that wire during a subsequent functional test.

Checking for cracked die is more complicated. Depending on where the die cracked, it is possible to have a cracked die and still have a major portion of the circuit work. As a result, we have to have vectors that exercise a good deal of each chip. Since most semiconductor manufacturers consider their test vectors to be proprietary, we must re-create vectors for each of the die in our Unify ASIC.

Another consideration is the number of pins available in the final package. As systems become more integrated, there tends to be fewer pins available. And that forces us into using a JTAG approach to testing. Higher pin counts allow us to make entire chips available at the pads for testing.

Performance checking depends on the nature of the Unify SiP. It might involve speed, analog circuitry, RF, or some combination of the above. In general, we will need to construct a tester interface board with the capability to accurately measure the Unify SiP.

Cost of a Unify SiP

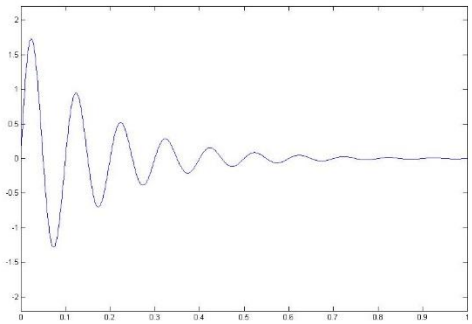
The cost of a Unify SiP will vary, depending on the components used within it. Tekmos uses a pricing model similar to contract manufacturers who build PC boards with standard products.

There are many stories of companies spending $20M or more to make an ASIC. And some of these stories are true. But an ASIC does not have to be expensive. The Tekmos approach of unifying existing parts with a technology appropriate ASIC in a stacked die package will reduce the cost substantially. Our graduated approach to NREs allows the initial parts to be made with engineering lots or shuttle runs, which reduces the initial investment, and allows initial production without high volume commitments.

Mixed Signal ASICs

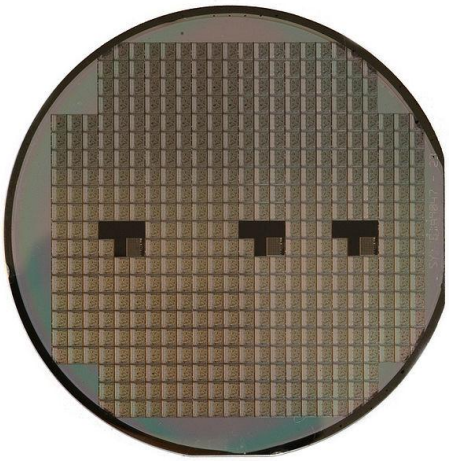
A **Unify** ASIC from Tekmos can include mixed signal circuitry. We can add the interface your design needs, to connect with the outside world. This can be sensor integration, additional power supplies, battery management, or signal conditioning.

Starting from a rich library of op-amps, voltage references, filters, charge pumps, and switches, we can provide the mixed solution that you need to succeed in the IoT market.



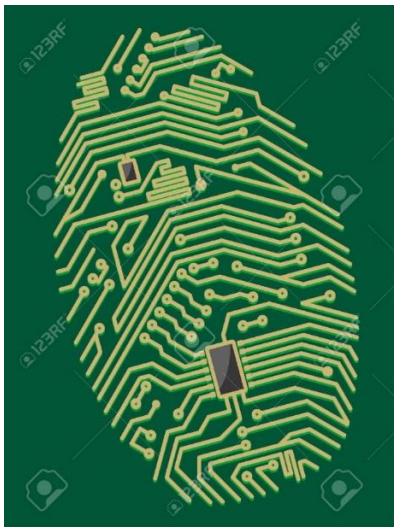
Technology

It is a fact that the NRE costs roughly double for each generation of fab technology. What is not so well understood is that the newest technology may not be required for all portions of the design. The stacked die approach of **Unify** ASICs allows Tekmos to mix technologies and use the most cost effective solution for each die in the stack. Thus the processor can be made in a 45 nm technology, while the ASIC itself can be made in a 180 nm technology. The key to a cost effective IoT solution is to just use the technology you need, but no more.



Design Security

There are two types of security issues in the IoT. The first involves hacker attacks, and these are typically dealt with by the processor. The other security issue is the security of the design itself. Any product made out of standard parts can be easily copied. But if the design includes a proprietary ASIC, then it becomes much more difficult to copy. And by working with Tekmos, the designer can be certain no one else has access to his design or to his Unify ASICs without his permission.



Engineering Resources

Chip design requires a lot of specialized knowledge, and access to a lot of expensive tools. That is the job of Tekmos. The customer only needs to define their system in RTL, and to have verified their design in a prototype, which is usually an FPGA. We will do the rest. We will need some access to the system designer, and to have the customer participate in periodic design reviews.

Ramping Up Production

With a new product development, it is common for the design to change, particularly after the product has had its first exposure to customers. What sounds great in a marketing meeting may need adjustments to achieve customer acceptance. This is why Tekmos offers the ability to run engineering lots or shuttle runs on the initial silicon. This is a great way to produce 100s or 1000s of parts without a large investment in photomasks. Then, when the product has reached market acceptance, we can invest in a full mask set to support high volume and lowest cost.

Unify With Tekmos

Contact us and learn how a Unify ASIC from Tekmos can launch your product into the IoT marketplace.

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Revision History

Date	Revision	Description
2/04/2016	1.0	Initial release
7/1/2016	2.0	Expand to 8 pages, add design flow

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