Port Replacement Unit (PRU)

For 6811 – type microprocessors

Features

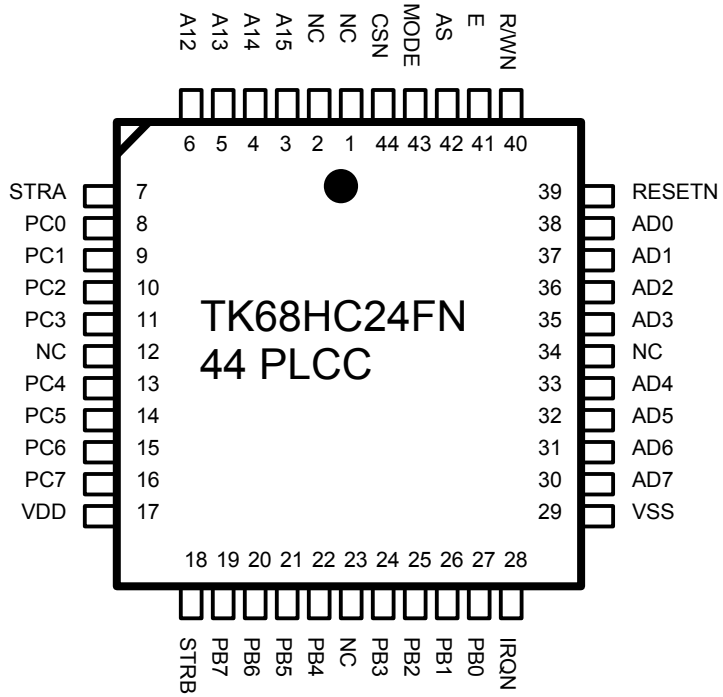
- Exact replacement for the Motorola MC68HC24 PRU
- Utilizes the Tekmos 6824 Core
- Replaces ports B and C of 6811 type microprocessors.
- The chip-select function allows multiple TK68HC24s to be used in systems requiring multiple parallel ports.
- 3 – 5.5 Volt Operation.
- 0 – 5 MHz Operation.
- Supports all handshake and I/O modes.
- Available in 40 PDIP (P) and 44 PLCC (FN) versions.

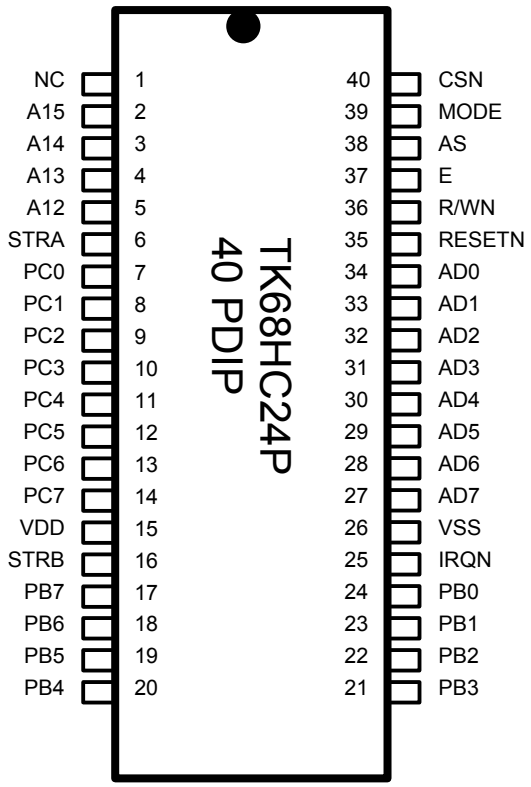
Description

The TK68HC24 is an exact replacement of the Motorola 68HC24.

The TK68HC24 is designed to replace the Port B and Port C functions of 6811 – type microprocessors. These functions are lost when the 6811 type microprocessors are operated in the expanded mode. The TK68HC24 has an address re-mapping feature that allows multiple TK68HC24s to be used within a single system.

Pinout





Pinout

PDIP 40	PLCC 44	Name	Type	Function
1	2	IOTEST	N / C	Not used in the Tekmos design
2-5	3-6	A15 – A12	Input	Address lines for port mapping.
6	7	STRA	Input	Handshake input
7-14	8-11, 13-16	PC0 – PC7	Bidirectional	General purpose input / output port
15	17	VDD	Supply	Positive supply
16	18	STRB	Output	Handshake output
17-24	19-22, 24-27	PB7 – PB0	Output	General purpose output port
25	28	IRQN	Output	Interrupt Request, open drain, active low
26	29	VSS	Supply	Ground
27-34	30-33, 35-38	AD7 - AD0	Bidirectional	Multiplexed address / data bus from the 68HC11
35	39	RESETN	Input	Reset, active low
36	40	RWN	Input	Read / Write control signal
37	41	E	Input	Enable – clock
38	42	AS	Input	Address strobe
39	43	MODE	Input	Selects operating mode at reset.
40	44	CSN	Input	Chip select

Pin Descriptions

IOTEST

No Connect

The IOTEST pin was removed from the 68HC24 design several years ago. However, it continued to be referenced on the data sheet. This pin is a true no connect, and may be either tied to a convenient supply, used for routing other signals, or it may be left floating.

A15 – A12

High Order Address - Inputs

These are the high order address lines from the processor. They are latched by the rising edge of the E clock. The value on the address lines is compared against the contents of the INIT register. A match, combined with an active chip select selects the part during the current bus cycle.

AD7 – AD0

Address and Data Bus - Bidirectional

These pins are a multiplexed address / data bus. During the first portion of the bus cycle, when the E clock is low, the AD bus contains the address. The address is strobed into an internal address latch by the ALE pin. During the second portion of the bus cycle, when the E clock is high, the AD pins carry data. Depending on the state of the RWN pin, the part will either read the bus, or drive the bus.

STRA

Strobe A – Input

This pin is used as an input handshake signal by Port C. In the simple strobed and input handshake modes, STRA is used to latch data into the PORTCL register. In the output handshake mode, STRA is used to acknowledge the output data. The EGA bit in the PIOC register controls which edge of STRA is active.

STRB

Strobe B - Output

The STRB pin serves as an output strobe for Port B when the part is operating in the simple strobed I/O mode. In the handshake mode, STRB is a handshake output line. In the input handshake mode, the pin serves as a READY line, inhibiting the external device from strobing data into Port C. In the output handshake mode, STRB indicates that new data has been written to Port B by the

processor. The PLS bit of the PIOC register controls whether this pin pulses or remains at a level.

PB7 – PB0

Port B, Bits 7 to 0 - Outputs

An 8 bit, general purpose output port. STRB pulses with each write to Port B in the simple strobed mode of operation.

PC7 – PC0

Port C, Bits 7 to 0 - Bidirectional

This is a general purpose, 8-bit bidirectional port. Each bit may be individually programmed by the DDRC register to be either an input or an output. Input data is read from the PORTCL register, while output data is written to the Port C register. The STRA pin serves as a handshake signal for this port.

IRQN

Interrupt Request – Open drain, active low output

This pin provides the interrupt signal back to the processor. It is a logical NAND of the STAF and STAI bits in the PIOC register.

AS

Address Strobe - Input

This pin serves to de-multiplex the address form the data on the AD bus. The falling edge of AS causes the address to be latched internally within the TK68HC24.

MODE

Mode Select - Input

The mode select pin is sampled at the rising edge of reset. A zero puts the chip into a special emulation mode, while a one leaves it in the normal operating mode.

CSN / Chip Select

Input, active low

This is the device chip select. The TK68HC24 is selected when 1) CSN is low, 2) the contents of the INIT register match address lines A12 – A15, and 3) when the lower order address lines (AD0 – AD7) select an internal register. The CSN signal is latched on the rising edge of the E clock.

RWN

Read / Write - Input

Determines whether data is being read from, or is being written to the device.

E

Enable - Input

The E (Enable) pin is the clock for the TK68HC24. The E clock runs at the external bus rate of the 6811 microprocessor.

RESETN

Active Low Input

The RESETN pin provides a synchronous reset to the part. It must remain low for 2 E clock cycles in order to be recognized.

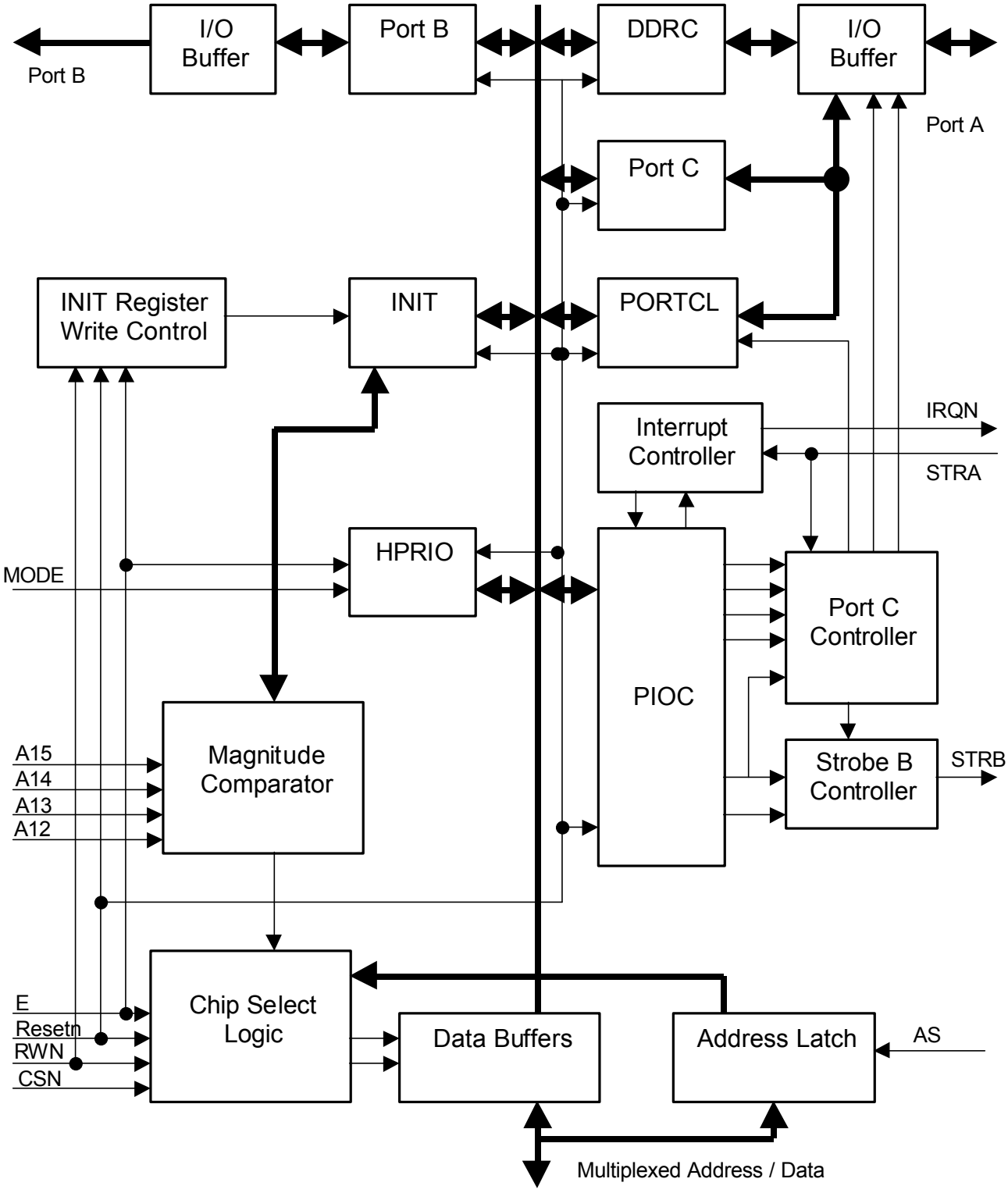


Figure 1. Block Diagram

Register Bit Map

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIOC	xx02	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB
PORTC	xx03	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
PORTB	xx04	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
PORTCL	xx05	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
DDRC	xx07	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
HPRIO	xx3C	-	SMOD	-	IRV	-	-	-	-
INIT	xx3D	-	-	-	-	REG3	REG2	REG1	REG0

Internal Register Addressing

A 64-byte address space is reserved for internal register access, although not all 64 addresses are used. The ABSOLUTE locations where these addresses will appear are specified by the reset initialization software and chip select logic provided by the end user (see INIT register).

Internal Register Bit Descriptions

The following list summarizes the registers, the bit mnemonics and their associated functions.

PARALLEL I/O CONTROL REGISTER (PIOC)

Reset value = 00000011

The PIOC register controls both the register handshaking and the modes of Port C.

STAF – Bit 7, Read only.

The STAF (strobe A Interrupt status flag) bit is set when a selected active edge is detected by the STRA input pin. This bit is ANDed with the STAI bit (b6) to generate interrupts (IRQN). This bit is cleared by reset to indicate no interrupt request is pending.

There is an automatic clearing mechanism on STAF which depends on the operating mode selected. There are three basic strobed modes, controlled, by the HNDS OIN bits.

When HNDS is zero, the simple strobed mode is specified and the OIN bit has no meaning or effect. In this mode, STAF flag is automatically set by detection of the selected edge on the STRA input pin indicating that new data is available in the Port C latch. The STAF flag is automatically cleared by a read of the PIOC register (with STAF set) followed by a read of the PORTCL latch register.

When HNDS is one and OIN is zero, the input handshake mode is specified. In this mode, the STAF flag is automatically set by detection of the selected edge on the STRA input pin indicating that new data is available in the Port C latch. The STAF bit is automatically cleared by a read of the PIOC register (with STAF set) followed by a read of the PORTCL latch register.

When HNDS is one and OIN is one, the output handshake mode is specified. In this mode, the STAF flag is automatically set by detection of the selected edge on the STRA input pin indicating that data from Port C has been accepted by the external system. The STAF flag is automatically cleared by a read of the PIOC register (with STAF set) followed by a write to the PORTCL latch register.

STAI – Bit 6, Read / Write

The STAI (strobe A interrupt enable mask) bit is used to specify whether or not a hardware interrupt sequence is to be requested whenever STAF is set. To request a hardware interrupt, both the STAI interrupt enable bit and the STAF flag bit must be set. This bit is cleared by RESET so that parallel I/O interrupts are inhibited. If this bit is set, an interrupt (IRQN) will be generated every time the SFAF bit is set.

CWOM - Bit 5, Read / Write

When the CWOM (Port C wire-OR mode) bit is zero, the Port C output pins operate normally. When this bit is set to one, the Port C outputs behave as open-drain type

drivers allowing wired-OR type external connections. When CWOM equals one, the top driver device is disabled so that pins may be driven low by writing zeros or become three-state by writing ones. With an external pull-up resistor, the non-driven lines are pulled to logic ones.

This permits Port C output pins to be safely wired in parallel with similar CMOS output drivers without fear of contentions which could otherwise cause destructive latch-up. This bit is cleared by RESET so Port C pins which are configured as outputs will operate normally.

Note that even when in the wired-or mode, the input protection diodes are still there, and so input voltages must never exceed VDD.

HNDS – Bit 4, Read / Write

When HNDS (handshake mode) bit is clear, the STRA pin acts as a simple input strobe to latch incoming data into the PORTCL latch register and the STRB pin acts as a simple output strobe that pulses after any write to Port B. When HNDS is set, it specifies that a handshake protocol involving Port C, STRA, and STRB is in effect. In all modes, STRA is an edge-sensitive input and STRB is an output. This bit is cleared by RESET. The strobe and handshake modes are described in greater detail in I/O PORTS.

OIN – Bit 3, Read / Write

The OIN (output or input handshake) bit has no meaning or effect unless HNDS is set to one. When this bit is zero, input handshake protocol is specified. When this bit is a one, output handshake protocol is specified. See I/O PORTS for a more detailed description of the handshake protocols.

PLS – Bit 2, Read / Write

The PLS (pulse/interlocked handshake) bit has no meaning or effect unless HNDS is set to one. When this bit is zero, interlocked handshake operation is specified. When this bit is one, pulse mode handshake operation is specified.

In interlocked modes, the STRB output line, once activated, remains active indefinitely until the selected edge is detected on the STRA input line. In pulse modes, the STRB output line, once activated, remains active for only two MCU E-clock cycles and then automatically reverts to the inactive state. This bit is cleared by RESET. For more details on the handshake protocols, see I/O PORTS.

EGA – Bit 1, Read / Write

The EGA (active edge for STRA) bit is used to specify which edge (rising or falling) on the STRA input pin is to be considered the active edge. When this bit is zero, the active edge is the falling edge and when this bit is one, the active edge is the rising edge. This bit is set to one by RESET.

When output handshake mode is specified, this bit is used to control the PORTC three-state variation as well as select the active acknowledge edge. In the three-state variation, the EGA bit specifies the trailing edge polarity for the STRA input pin which is interpreted as the enable/acknowledge signal. Assertion of STRA overrides the DDRC specifications to force Port C to be outputs and the edge of negation is the active edge acknowledge command.

If EGA is zero, the falling edge at STRA is the active edge which causes STAF to be set and STRB to be negated. Additionally, if EGA is zero, Port C bits obey the DDRC specification while STRA is low but Port C is forced to be an output when STRA is high.

If EGA is one, the rising edge of STRA is the active edge. This causes STAF to be set and STRB to be negated. In addition, Port C bits obey the DDRC specification while STRA is high, but Port C is forced to be an output when STRA is low.

INVB – Bit 0, Read / Write

The INVB (Invert Strobe B) bit is used to specify whether or not to invert the normal strobe B (STRB) logic output levels. When this bit is one, no inversion is specified and the active level on the strobe B output line is logic one. When this bit is zero, inversion is specified and the active level on the

strobe B output line is logic zero. This bit is set to one by RESET so that the STRB output will initially be in the low state out of reset. For a more detailed description of the handshake protocols, see the I/O PORTS section.

PORT C DATA REGISTER (PORTC)

Reset value = 00000000

Port C (PORTC) is a general purpose input/output Port Complemented by full handshake capability. For bits that are configured as inputs, reads of this address return the level sensed at the pin. For bits configured as outputs, reads return the level sensed at the input to the pin driver. When a Port C pin is being used for the three-state variation of parallel output handshake, reads return the level sensed at the input to the pin driver even if the DDR bits suggest that the pin is configured as an input.

Writes to Port C cause the value to be latched in the 8-bit Port C data register. (Note that this is not the same register as the PORTCL latch register described later.) When the corresponding DDRC bit is set, the value in the Port C data register is driven out of the Port C pin. This data latch allows the programmer to initialize the data prior to turning on the output drivers by setting bits in the DDRC. The PORTC register is cleared by RESET.

The Port C bits are labeled as PC7 – PC0.

PORT B DATA REGISTER (PORTB)

Reset value = 00000000

Port B (PORTB) is a general purpose output-only port. Reads of this address return the level sensed at the input to the pin driver. Writes to Port B cause the value to be latched in the 8-bit Port B data register. The PORTB register is set to zero by RESET.

The Port B bits are labeled as PB7 – PB0.

PORT C LATCHED DATA REGISTER (PORTCL)

Reset value = XXXXXXXX (not reset)

The Port C latch register (PORTCL) allows alternate access to Port C information. This register is used in conjunction with the strobed parallel I/O modes. Input data is latched into the PORTCL register on each selected edge on the STRA pin. The latched data is the level at the pins regardless of the operating mode selected. Reads of PORTCL return the contents of the Port C input latch. Reads also act as part of an automatic flag clearing sequence in the input handshake modes of Port C.

Writes to the PORTCL register are equivalent to writes to the PORTC register except the PORTCL writes are used as part of an automatic flag clearing sequence in the output handshake modes of Port C. For more information on the Port C strobed and handshake modes, see **I/O PORTS**. The contents of PORTCL are not affected by RESET.

The Port CL bits are labeled as PCL7 – PCL0.

DATA DIRECTION REGISTER C (DDRC)

Reset value = 00000000

The data direction register C (DDRC) is a read/write register used in conjunction with Port C to specify the direction of data flow at each of the Port C pins. A Port C pin is an input if the corresponding bit in DDRC is zero. The pin is an output if the corresponding bit in DDRC is set to one. During reset, all bits in the DDRC are cleared to zero. The effects of DDRC are overridden in the three-state variation of the output handshake mode. For additional information, see **I/O PORT OPERATION, Output Handshake Protocol, Three-State Variation**.

The port bits are labeled as DDRC7 – DDRC0.

HIGHEST PRIORITY INTERRUPT REGISTER (HPRIO)

Reset value = 0*0*0000

Note that the reset condition of SMOD and IRV depends on initialization mode.

SMOD – Bit 6, Read / Write once

The SMOD (Special Test Mode) bit is a read only bit which reflects the operating mode of the peripheral as selected by the MODE input. The inverted state of MODE is latched in SMOD by the rising edge of RESET. When SMOD equals zero (MODE equals one), the peripheral is operating in normal mode. When SMOD equals one (MODE equals zero), the special test mode is selected.

The special test mode may be exited under software control by writing SMOD from a one to a zero. However, the special test

mode may not be re-entered by writing the bit back to one. This SMOD bit becomes write-protected once written to zero. This implies that the normal operating mode can be entered either through a hardware reset or through software while the special test mode may only be entered through hardware reset.

IRV – Bit 4, Read, write once

The IRV (Internal Read Visibility) control bit eliminates potential bus conflict problems when this device is used in conjunction with the 68HC11. To allow a logic analyzer to monitor the internal bus activity of the 68HC11, provisions have been made for the MPU to selectively drive the external data bus during internal reads as well as writes. The selection of this feature is controlled by the IRV bit.

The state following reset and the programming characteristics of the TK68HC24 IRV bit are the same as the 68HC11 IRV bit. However, the functional characteristics are the opposite. The TK68HC24 IRV functions as follows:

Logic 0 – Reads of the INIT and HPRIO registers will enable the multiplexed address/data buffers, placing the contents of the selected register on the bus.

Logic 1 – Reads of the INIT and HPRIO registers do not enable the multiplexed address/data bus drivers.

This bit may be read at any time, although the multiplexed address/data bus will remain high-impedance during reads when IRV equals one. Only one write will be acknowledged and then only if SMOD equals one. The IRV bit is forced to zero (reads of HPRIO and INIT enabled) when SMOD is written from a one to a zero (entering normal mode). Resets clears this bit in the normal mode and sets this bit in the special test mode.

b7, b5, b3, b2, b1, b0 – Not Implemented

These bits are not implemented. Writes have no meaning or effect on them. Reads of these bits will always return a logic zero value.

INIT (I/O MAPPING REGISTER)

Reset value = 00000001

The INIT (I/O Mapping) register is a special purpose 8-bit register that is used (optionally) during initialization to change the default locations of the TK68HC24 internal registers in the MPU/MCU memory map. The lower four bits of the TK68HC24 INIT register are duplicates of the 68HC11 INIT register. These four bits are used to specify the active state of the four high order address bits to the register address decoding logic. This register functions identically to the 68HC11 INIT register with the following exceptions: 1) only the lower four bits are implemented, and 2) the protection mechanism is not time dependent.

The default starting address of the 64-byte internal register space is $1x00 (i.e. INIT is initialized to $01). Initialization software can move registers to any 4K boundary within the memory map. External decoding of A8 through A11 specifies where in the 4K block (on 256-byte boundaries) the 64-byte register space is located. As an example, assume that the initialization software wrote the value $09 to the INIT register and that CS was true when A8 through A11 were low. This would place the registers from $9000 through $903F in the memory map. Decoding A8 through A11 so that the chip is selected when all four address lines are low maps the TK68HC24 registers to the same address as the 68HC11 registers.

The INIT register is special in that there is a write-protect mechanism associated with it. In the normal mode, the register may be written once at any time after reset. This differs from the operation of the 68HC11 INIT register which becomes write protected after the first 64 E-clock cycles, whether or not a write to the register has occurred. After the first write, the INIT register becomes write-protected and thereafter is a read-only register.

While in the special test mode (SMOD equals one), the protection mechanism is overridden and the INIT register may be written repeatedly as long as SMOD remains a one. When SMOD is written to a zero (to enter the normal operating mode), the write-protect mechanism is enabled. One additional write, regardless of the number of writes performed while in the special test mode, is allowed after entering normal operating mode. The upper four bits of the INIT register are unused, and will always read as zeros.

I/O Port Operation

There are two 8-bit parallel I/O ports on the TK68HC24. Port B is a general purpose output-only port. Port C may be used as general purpose input and/or output pins, as specified by the DDRC register. In conjunction with STRA and STRB, ports B and C may be used for special strobed and handshake modes of parallel I/O as well as general I/O.

Fixed Direction I/O (Port B)

Port B is a general purpose output-only port. The data direction is fixed in order to properly emulate the operation of the 68HC11 Port B. Reads of Port B return the levels sensed at the input of the pin drivers. Write data is stored in an internal latch which directly drives the output pin driver. Reset clears the data register, forcing the outputs low.

General Purpose I/O (Port C)

When used as a general purpose I/O port, each pin has associated with it one bit in the Port C data register and one bit in the corresponding position in the data direction register (DDRC). The DDRC is used to specify the primary direction of data on the I/O pin. However, specification of a line as an output does not disable the ability to read the line as a latched input.

When a bit which is configured as an output is read, the value returned will be the value at the input to the pin driver. When a pin is configured as an input (by clearing the DDRC bit) then pin becomes a high-impedance input. When writing to a bit that is configured as an input, the value will not affect the I/O pin. However, the bit will be stored in the PORTC latch, and will drive the pin should the DDRC register ever be set.

This operation can be used to preset a value for an output port prior to configuring it as an output, so that glitches of an output state which are not defined for the external system may be avoided.

Reset configures the port for input by clearing both the DDRC and PORTC registers.

Simple Strobed I/O

The simple strobed mode of parallel I/O is selected when the HNDS bit in the PIOC (Parallel I/O Control) register is clear. This mode forces PORTCL to be a strobed input port with the selected edge of the STRA pin used to latch the data. Port B becomes a strobed output port with the STRB pin acting as the output strobe.

Strobed Input Port C

Even in the input mode, the DDRC register still controls the direction of the Port C pins. As a result, if a bit in the DDRC register is set, that bit still acts as an output from the Port C register.

Depending on the edge selected by the EGA bit in the PIOC register, either the positive edge (EGA = 1) or the negative edge (EGA = 0) of the STRA strobe will latch the values on the Port C pins into the PORTCL register. The action will also set the STAF bit in the PIOC register.

If the STAI bit in the PIOC register is also set, then an interrupt sequence is requested in the IRQN pin. The STAF flag is automatically cleared by reading the PIOC register (with STAF set), followed by a read of the PORTCL register. Additional active edges of the STRA pin will continue to latch new data into the PORTCL register, regardless of the state of the STAF flag. Consecutive active edges of the STRA signal must be a minimum of two E-clock cycles apart.

Reads of the PORTCL register return the last value latched. Reads of the PORTC register return either the in value for inputs or the contents of the PORTC register for outputs.

Strobed Output Port B

In this mode, the STRB pin is a strobe output which is pulsed each time there is a write to Port B.

FULL HANDSHAKE I/O

The full handshake modes of parallel I/O use Port C, the DDRC port, STRA, and STRB. There are the two basic modes of input and output, and an additional variation on the output handshake mode that allows for three-state operation of Port C. In all handshake modes, STRA is an edge detecting input and STRB is a handshake output line.

Input Handshake Protocol

In the input handshake mode, Port C is a latching input port, STRA is an edge-sensitive latch command from the external system that is driving Port C and STRB is a READY output line controlled by logic in the TK68HC24.

In a typical system, an external device wishing to write to Port C would test the READY line (STRB). When a ready condition was recognized, the external device would place data on the Port C inputs and then pulse the STRA input to the TK68HC24. The active edge on the STRA line would latch the Port C data into the PORTCL register, set the STAF flag (optionally causing an

interrupt), and deassert the READY line (STRB). Deassertion of the READY line would automatically inhibit the external device from strobing new data into Port C. Reading the PORTCL latch register, after reading PIOC with STAF set, clears the STAF flag. Whenever PORTCL is read, the READY (STRB) line is asserted indicating that new data may now be strobed in to Port C.

The STRB line can be configured (with the PLS control bit) to be a pulse output (pulse mode) or a static output (interlocked mode). The only difference between the pulse and interlock modes is that in pulse mode, the READY line pulses (asserts) for only two E-clock periods after the latched data becomes available. While in interlock mode, the asserted state of the READY line lasts until new data is strobed into Port C via the STRA input line.

The Port C DDR bits should be cleared (input) for each bit that is to be used as a latched input bit. It is, however, possible to use some Port C bits as latched inputs with the input handshake protocol and at the same time use other Port C bits as static inputs and still other Port C bits as static output bits.

The input handshake protocol has no effect on the use of Port C bits as static inputs or static outputs. Reads of the PORTC register always return the static logic level at the Port C pins (for lines configured as input) or at the inputs to the pin drivers (for lines configured as outputs). Data latched into PORTCL always reflects the level at the Port C pins. Writes to either the PORTC address or the PORTCL address will write information to the Port C output register without affecting the input handshake strobes.

NOTE:

After programming PIOC to enter the input handshake mode, STRB will remain in the inactive state. The precaution has been taken to ensure that the external system will not strobe data into PORTCL before all initialization is complete. When ready to accept data, the MPU/MCU should perform a dummy read of the PORTCL address. This operation will assert STRB initiating the input handshake protocol.

Output Handshake Protocol

In the output handshake scheme, Port C is an output port, STRB is a READY output, and STRA is an edge-sensitive acknowledge input signal indicating that Port C output data has been accepted by the external device. In a variation of this output handshake operation, STRA is used as an output enable input as well as an edge-sensitive acknowledge input.

In a typical system, the controlling processor writes to the TK68HC24, placing data in the Port C output latch. Stable data on the Port C pins is indicated by the automatic assertion of the TK68HC24 READY (STRB) line. The external device then processes the available data and pulses the STRA input to indicate the new data may be placed on the Port C output lines. The active edge on STRA causes the READY (STRB) line to be automatically deasserted and the STAF status flag to be set (optionally causing an interrupt). In response to STAF being set, the program puts out new data on Port C as required.

There are two addresses associated with the Port C data register, the normal PORTC data address and a second address (PORTCL) that accesses the input latch on reads and the normal port on writes. On writes to the second address (PORTCL), the data goes to the same port output register as it would on a write to the PORTC address but the STAF flag bit is cleared (provided PIOC was first read with the STAF bit set). This allows an automatic clearing mechanism in output handshake modes to co-exist with normal Port C outputs.

All eight bits in Port C must be used as outputs while the output handshake protocol is selected. That is, part of Port C may not be used for static or latched inputs while the remaining bits are being used for output handshake. The following paragraphs cover this limitation in more detail.

Output Handshake Protocol, Three-State Variation

There is a variation to the output handshake protocol that allows three-state operation of Port C. It is possible to directly interconnect this 8-bit parallel port to other 8-bit three-state devices with no additional external parts.

The STRA signal is used as an acknowledge/enable input whose sense is controlled by the EGA bit in the PIOC register. The EGA bit specifies the transition from the asserted to the deasserted state of the STRA Input signal. If EGA is zero, the asserted state is high and falling edges are interpreted as acknowledge signals. If EGA is one, the asserted state is low and rising edges are interpreted as acknowledge signals.

As long as the STRA input pin is negated, all Port C bits obey the data direction specified by DDRC. Bits which are configured as inputs (DDR bit equals zero) will be high impedance. When the STRA

input is asserted, all Port C lines are forced to be outputs regardless of the data in DDRC.

This operation limits the ability to use some Port C bits as static inputs while using others as handshake outputs. However, it does not interfere with the use of some Port C bits as static outputs while others are being used as three-state handshake outputs. Port C bits which are to be used as static outputs or normal handshake outputs should have their corresponding DDRC bits set. Bits which are to be used as three-state handshake outputs should have their corresponding DDRC bits clear.

Interaction of Handshake and General Purpose I/O

There are two addresses associated with the Port C data register: the normal PORTC address and a second address (PORTCL) that accesses the input latch on reads and the normal port on writes. On writes to the second address (PORTCL), the data goes to the same port output register as it would on a write to the port output address. When operating in the output handshake mode, writing to PORTC will not clear the STAF bit whereas writing to PORTCL will clear it. This allows an automatic clearing mechanism to co-exist with normal Port C outputs.

When full input handshake protocol is specified, both general purpose input and/or general purpose output can co-exist at Port C. However, the three-state feature of the output handshake mode interferes with general purpose inputs in two ways.

First, in full output handshake, the Port C pins are forced to be driven outputs during any period in which STRA is in its active state regardless of the state of the DDRC bits. This potentially conflicts with any device trying to drive Port C unless the external device has an open-drain type output driver.

Secondly, the value returned on reads of Port C is the state at the inputs to the pin drivers regardless of the state of the DDRC bits. This allows data written for output handshake to be read even if the pins are in a three-state condition.

The following is an example of Port C being used for full input handshake, general purpose input, and general purpose output all at the same time. Assume that the PIOC and DDRC control registers are set up as follows:

PIOC = 0111_0000

DDRC = 0000_1100

In this example, Port C bit b7 through b4 will be used for input handshake, bits b3 and b2 will be used as open-drain type general purpose outputs, and bits b0 and b1 will be used as general purpose inputs. The DDRC register is configured such that bits b2 and b3 are outputs and the rest of the Port C bits are inputs. The PIOC register is configured such that full-input handshake is specified (HNDS equals one and OIN equals zero), CWOM equals one so any pins in Port C which are configured as outputs will behave as open-drain type outputs. The other bits in PIOC are not important for the discussion of this example.

When data is latched into PORTCL according to the input handshake protocol, all eight bits are captured although only the four MSBs are of interest to the input handshake software. The data latched into all eight bits of PORTCL will be the levels present at Port C pins.

Software driving the bits b2 and b3 general-purpose outputs would perform writes to PORTC which would not affect the handshake protocol or the latching of data into PORTCL. Data written to Port C bits b0, b1, and b4 through b7 would also be latched into the internal Port C output latch but since the corresponding DDRC bits are zeros, the corresponding Port C pins would remain unaffected.

Bit manipulation and read-modify-write instructions could be used on PORTC because reads of PORTC do not affect the input handshake functions. Although writes to PORTCL would also cause data to be written to Port C, this address should not be used for general purpose output. This is because bit manipulation and read-modify-write instructions read the location before writing to it and this read would interfere with the input handshake protocol.

Finally, to use bits 0 and 1 for general purpose inputs, simply read PORTC which will return the desired information and will not interfere with the input handshake protocol. Note that the current state of the Port C bits b4 through b7 are also read; therefore, even the pins which are being used for input handshake can be read at any time without disturbing the input handshake function.

SYSTEM CONFIGURATION

The TK68HC24 allows an end user to configure the peripheral to his specific MCU system through the use of hard wired options such as the mode select pin (MODE) and by the use of internal registers under software control. The following section describes those options which are fixed through hardware. Other configuration options, which can be changed dynamically, are discussed in the sections entitled I**/O PORTS and MODES OF OPERATION**.

MODE SELECTION

A dedicated mode select pin (MODE) determines which of two operating modes the TK68HC24 enters out of RESET. Both modes properly emulate the action of Ports B and C of the 68HC11. The modes are the normal and special test modes.

The state of the mode select pin (MODE) is latched into the peripheral by the rising edge of RESET with the inverse of the latched value reflected in the SMOD bit of the HPRIO register. Normal mode is indicated by SMOD equals zero (MODE equals one). Special Test mode is indicated by SMOD equals one (MODE equals zero). The difference between these two modes is limited to the operation of the INIT and HPRIO registers.

The MODE input corresponds (in function, but not voltage levels) to the MODB/VPGM input of the 68HC11. The 68HC11 requires either V_{DD} or a level 1.8 x V_{DD} on the MODB pin to select the operating mode; whereas, the TK68HC24 requires only logic level signals. The 1.8 x V_{DD} level required by the 68HC11 corresponds to a logic low on the TK68HC24. The V_{DD} level required by the 68HC11 corresponds to a logic high on the TK68HC24. In normal operation, the special test mode is not used and the mode pin on both the 68HC11 and the TK68HC24 can be tied to V_{DD}.

STATE AFTER RESET

When a low level is sensed on the RESET pin, the TK68HC24 enters the reset state. Most of the registers and control bits are forced to a specific state during reset and, if a user requires a different configuration, he must write the desired values into these registers in his initialization software. For detailed information about the options available, see INTERNAL REGISTER DESCRIPTION.

Note that RESET is synchronized to the system clock (E) before being used internally. For this reason, RESET must be held low for a minimum of two E-clock cycles to be recognized. Once recognized, the peripheral is initialized as described below.

Most of the configuration state after reset is independent of the selected operating mode. The STAF, STAI, and HNDS bits in the PIOC register are initialized to zeros so that no interrupt is pending or enabled and the simple strobed mode (rather than full handshake modes) of parallel I/ O is selected. The CWOM bit is initialized to zero (Port C not operating in wire-OR mode). Port C is initialized as a general purpose, high-impedance input port (DDRC equals $00), STRA as an edge-sensitive strobe input, and the active edge is initially configured to detect rising edges (EGA bit set to one by RESET). The STRB strobe output is initially a zero (INVB bit is initialized to one), while Port B is initialized with all outputs forced low.

The SMOD and IRV bits in the HPRIO register reflect the status of the MODE input at the rising edge of RESET. Reset also deselects the chip and forces the multiplexed address/data bus to high impedance inputs.

MODES OF OPERATION

SPECIAL TEST MODE

The special test mode is selected with MODE equal to zero at the rising of edge of RESET. Initialization into this mode loads HPRIO with $50 (SMOD and IRV equal one) and disables the INIT register write-protect mechanism.

While in special test mode (SMOD bit equals one), the INIT register write-protect mechanism is overridden and INIT remains writable as long as SMOD remains one. When SMOD is written to a zero (to enter the normal operating mode), the write-protect mechanism is enabled. One additional write is allowed after entering normal operating mode regardless of the number of writes performed while in the special test mode.

The reset state of IRV is one in the special test mode. An attempted read of either the INIT or HPRIO register with IRV equal to one will leave the data bus in a high impedance state with the output buffers disabled. If IRV equals zero, the data buffers are enabled and the contents of the selected register are placed on the data bus. The IRV bit is writable only one time while in the special

test mode. Entering the normal mode forces the IRV bit to zero, enabling the data bus output buffers on reads of these two addresses. Table 1 summarizes the chip select options.

Table 1. TK68HC24 Chip Select Action Summary

CSN	IRV	Action Taken
0	0	Chip selected, HPRIO and INIT reads enabled.
0	1	Chip selected. HPRIO and INIT reads disabled
1	X	Chip not selected

NORMAL MODE

Normal mode is selected when the MODE input is at a logic high level at the rising edge of RESET. The HPRIO register is initialized to $00 (SMOD and IRV equal zero). The INIT register write-protect mechanism is enabled, allowing only a single write to INIT. Reads of both the INIT and HPRIO register enable the output buffers, thus providing visibility into the contents of these registers. The HPRIO register is write-protected while in the normal mode. A reset sequence must be initiated to change the contents of this register.

NOTE

A write to the INIT register must be included in the initialization software whether or not the registers are to be relocated. This write will ensure that an accidental write to register at a later time will not cause the registers to be remapped. THIS IS ONE OF THE FUNCTIONAL DIFFERENCES BETWEEN THE 68HC11 PORTS AND THE TK68HC24 IMPLEMENTATION.

Differences Between the Motorola and Tekmos Version of the TK68HC24

1. The TK68HC24 is a new design, and is manufactured in a 0.8u CMOS process. The design has been modified to compensate for the faster process in order to retain compatibility with the older parts.
2. All inputs now have Schmitt triggers. Inputs fabricated on the new process will be faster. That makes them more sensitive to noise spikes, and they require faster rise times to avoid input oscillation. The insertion of Schmitt triggers on all inputs and bi-directional signals removes this sensitivity. The new parts still meet all of the original input level specifications.
3. Reset has been modified. In the original circuit, it was possible to trigger a partial chip reset by the presence of a well placed glitch on the reset line. The faster Tekmos implementation might respond to noise on the reset line that would not affect the original parts. The modification requires the presence of reset for at least 1/2 E clock before it is recognized. This is consistent with the specification, which requires users to keep the E clock low for two entire clock cycles.
4. The IOTEST pin has been removed from the documentation. This pin was not present on the old 68HC24s.

68HC11 And TK68HC24 Operational Differences

INIT REGISTER WRITE-PROTECT MECHANISM

The 68HC11 INIT register write-protect mechanism automatically disables writes to the INIT register 64 E clock cycles after the rising edge of RESET. The TK68HC24 write-protect circuitry IS NOT TIME DEPENDENT. Only a write to the INIT register will disable further writes. Both the 68HC11 and TK68HC24 INIT registers can be written repeatedly in the special test mode of operation (see SPECIAL TEST MODE) or once in the normal mode.

This difference dictates that the user should not rely on the timeout feature of the 68HC11 to write-protect the INIT register if he plans to utilize the same software with the TK68HC24. Instead, a write to the INIT register should be done during initialization, even if the remapping feature is not going to be used.

STRA PULSE WIDTH

Due to differences in implementation technology, the TK68HC24 incorporates an additional level of synchronization (over the 68HC11) on the STRA input. Under normal operating conditions, the end user will be unaware of this anomaly. Only systems which continually strobe new data into PORTCL are affected.

In order to allow the STRA signal to propagate through the internal feedback mechanism, a minimum delay of two E-clock cycles between active edges has been specified. This delay should not concern most users, since the time required to acknowledge the receipt of data and to read the data is much greater that two cycles.

STRB SYNCHRONIZATION

The 68HC11 synchronizes changes of Port B, Port C, and STRB data to an internal quadrature clock. This method of implementation makes internal buffer delays transparent to the end user. This internal clock is generated from the 4X clock, and as a result, cannot be duplicated by the TK68HC24. Port B and Port C data are synchronized to the E clock and become valid t_{PWD} after the falling edge of E instead of a setup time before the falling edge of E.

The most noticeable change involves STRB. The STRB signal is synchronized to the rising edge of E instead of the quadrature clock as in the 68HC11. At slow clock rates (much less than 1MHz), the delay between valid data on the port pins and the assertion of STRB could be considerable.

Maximum Ratings

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	Vdd	-0.5	7.0	V
Input Voltage	Vin	Vss – 0.5	Vdd + 0.5	V
Current Drain per Pin	Imax		25	mA
Operating Temperature Range	Ta	-40	85	°C
Storage Temperature range	Tstg	-55	+150	°C

DC Electrical Specifications (Vdd = 5.0 V +/- 10%, Vss = 0 V, Ta = -40°C to +85°C)

Characteristics	Symbol	Min	Max	Unit
Output Voltage (Iload = +/- 10 uA) All Outputs All outputs except IRQN (Note 1)	Vol Voh	- Vdd - 0.1	0.1 -	V
Output Low Voltage (Iload = 1.6 mA)	Vol	-	0.4	V
Output High Voltage (Iload = -0.8 mA, Vdd = 4.5 V) All outputs except IRQN (Note 1)	Voh	Vdd - 0.8	-	V
Input Low Voltage All inputs	Vil	Vss	0.2 x Vdd	V
Input High Voltage All inputs	Vih	0.7 x Vdd	Vdd	V
3-State Leakage (Vin = Vss or Vdd) PC0-PC7, AD0-AD7	Ioz	-	+/- 10	uA
Input Current (Vih = Vdd or Vss) E, AS, R/WN, CSN, MODE, A12-A15, STRA	Iin	-	+/- 1	uA
Total Supply Current (Note 2)	Idd	-	5	mA
Input Capacitance	Cin	- -	8.0 12.0	pF
Power Dissipation	Pd	-	25	mW

Note 1. IRQN is an open-drain output. Voh does not apply.
Note 2. Measured with Port C, CSN = 0 V., RESETN, MODE, R/WN = Vdd, reading Port 2 each cycle.

Mode Selection Electrical Characteristics (Vdd = 5.0 V +/- 10%, Vss = 0 V, TA = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
MODE Programming Voltage Low	Vmpl	0	-	0.2 x Vdd	V
MODE Programming Voltage High	Vmph	0.7 x Vdd	-	Vdd	V
RESETN Low Input Pulse Width	PWrstl	2	-	-	Ecyc
Mode Programming Setup Time	t_{MPS}	2	-	-	Ecyc
Mode Programming Hold Time	t_{MPH}	0	-	-	Ecyc

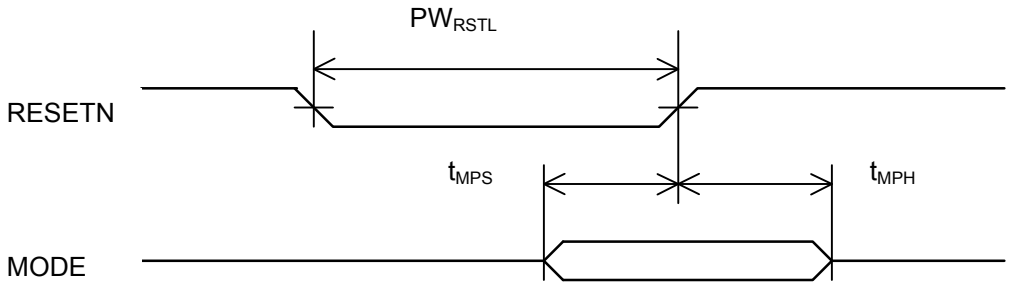


Figure 2. Mode Selection Timing

Peripheral Port Timing

(Vdd = 5.0 V ± 10%, all timing is shown with respect to 20% Vdd and 70% Vdd unless otherwise noted.)

Characteristics	Symbol	Min	Max	Unit	Fig. No.
Peripheral Data Setup Time (Post C)	t_{PDSU}	200	-	ns	4
Peripheral Data Hold Time (Post C)	t_{PDH}	10	-	ns	4
Delay Time, E Negative Transition to Peripheral Data Valid (Ports B and C, see Note 1)	t_{PWD}	-	100	ns	3
Input Data Setup Time (Port C)	t_{IS}	50	-	ns	6, 7
Input Data Hold Time (Port C)	t_{IH}	10	-	ns	6, 7
Delay Time, E Positive Transition to STRB Asserted (see Note 1)	t_{DEB}	-	80	ns	5, 8, 9
Delay Time, E Positive Transition to STRB Negated Handshake Mode (see Note 1)	t_{DEBN}	-	80	ns	7, 9
Setup Time, STRA Asserted to E Negative Transition (see Note 2)	t_{AES}	0	-	ns	7, 8, 9
Delay Time, STRA Asserted to Port C Data Out Valid (see Note 3)	t_{PCD}	-	100	ns	9
Hold Time, STRA Negated to Port C Data	t_{PCH}	10	-	ns	9
Three-State Hold Time	t_{PCZ}	-	150	ns	9
STRA Cycle Time	t_{Scyc}	2	-	E_{cyc}	6,7

Notes:
1. The method of calculating the timing for this characteristic differs from the 68HC11.
2. If this setup time is met, STRB will be acknowledged in the next cycle. If it is not met, the response will be delayed one more cycle.
3. Port C timing is only valid for active drive (CWOM bit is not set in PIOC).

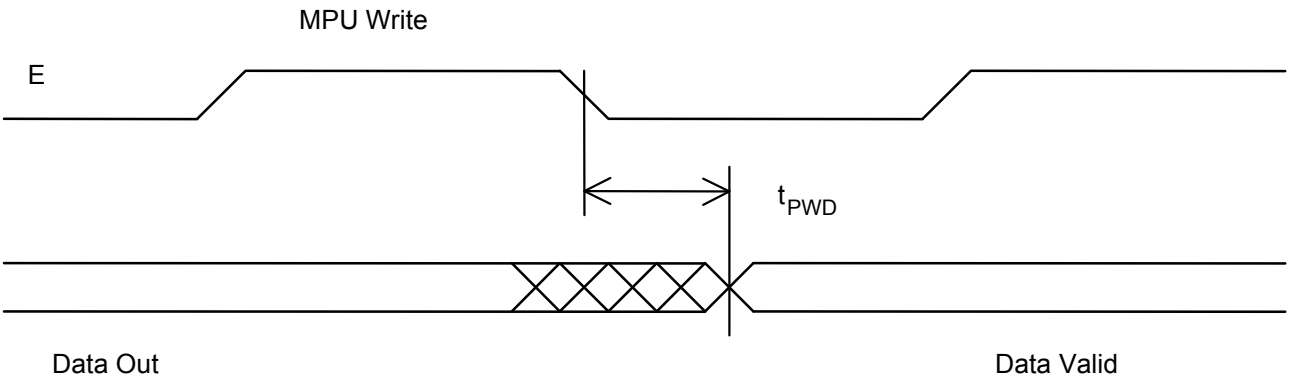


Figure 3. Port Write Timing

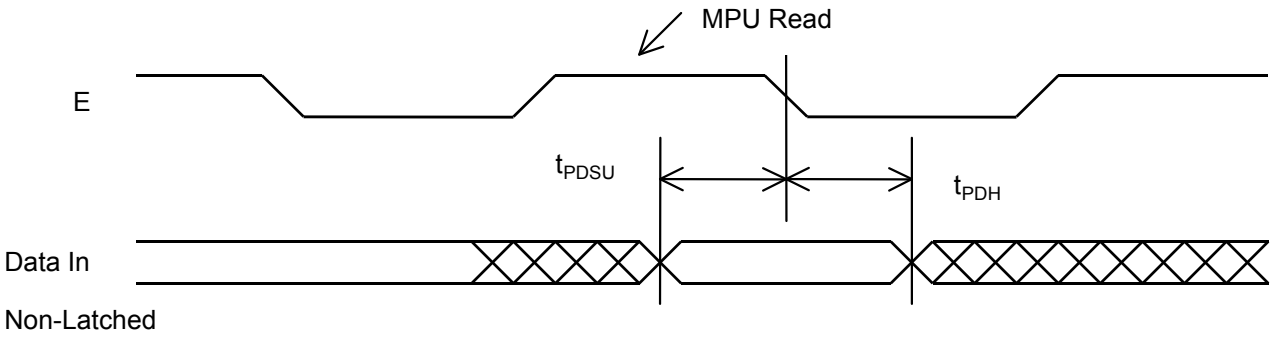


Figure 4. Port C Static Read Timing

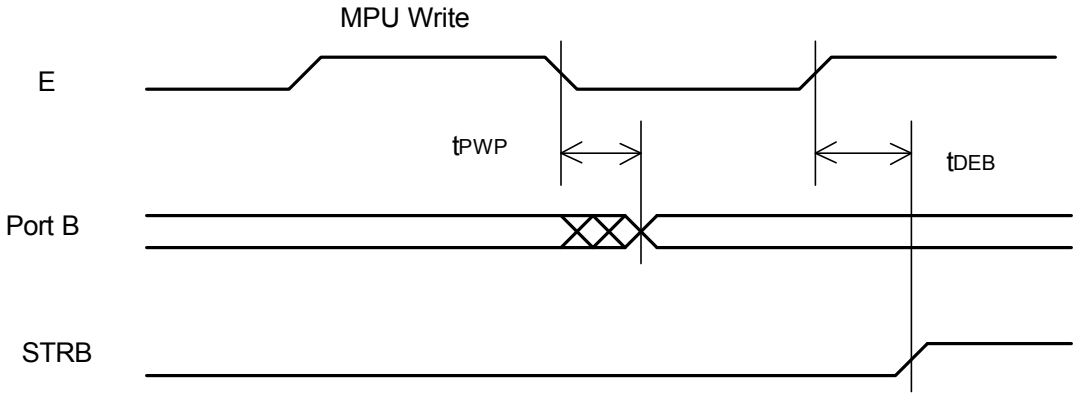


Figure 5. Simple Output Strobe Timing

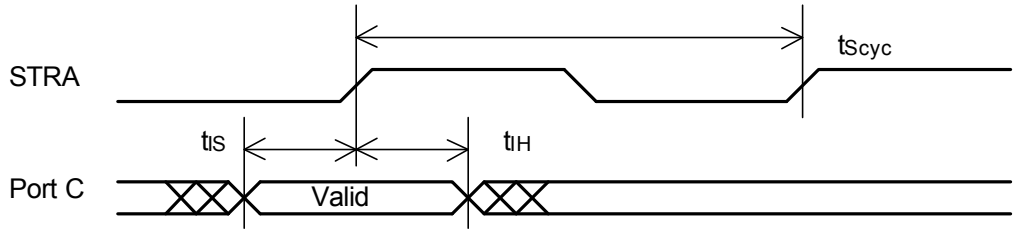


Figure 6. Simple Input Strobe Timing

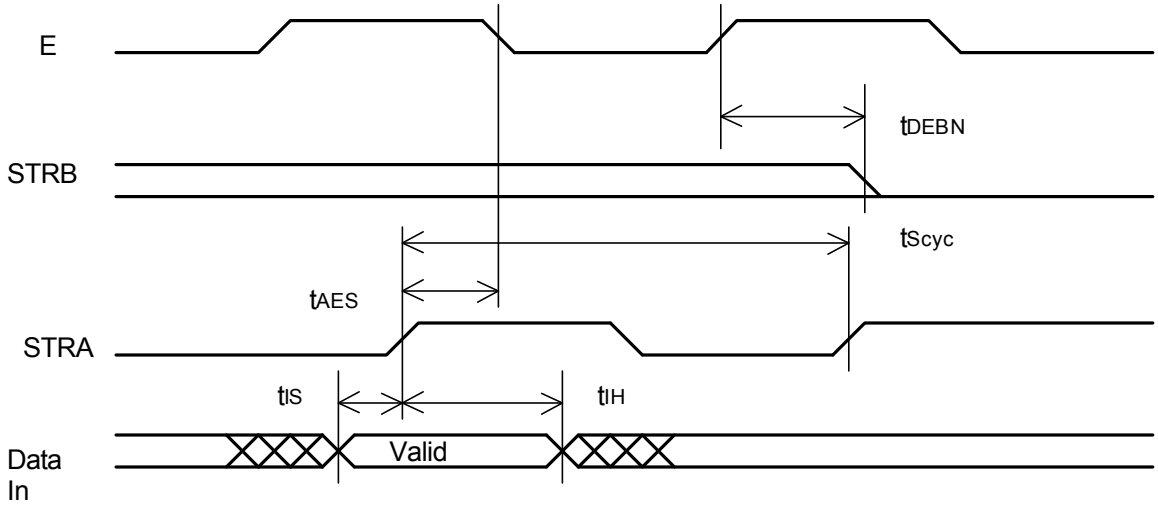


Figure 7. Port C Input Handshake Timing

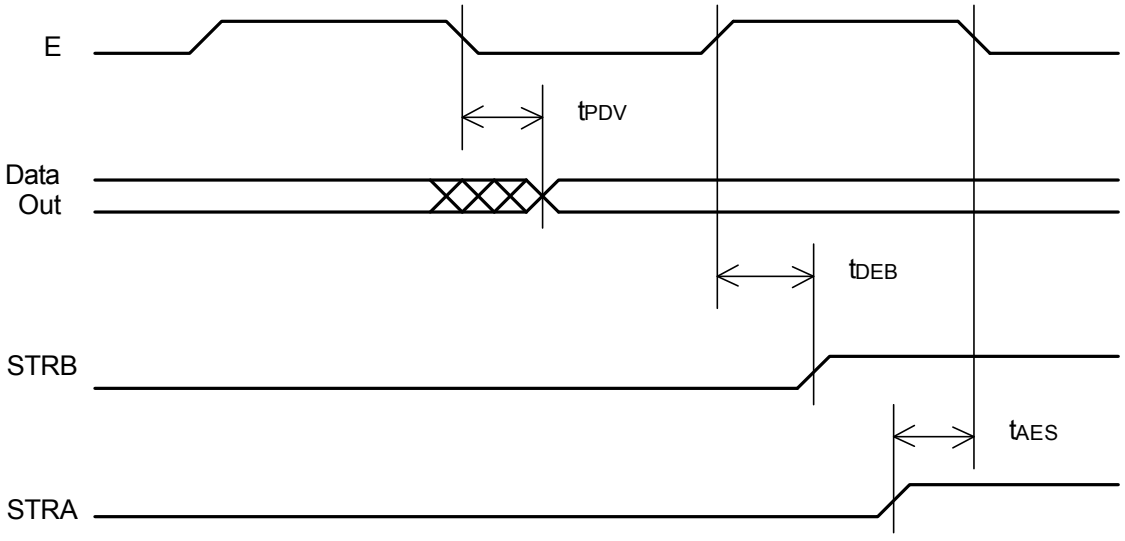


Figure 8. Port C Output Handshake Timing

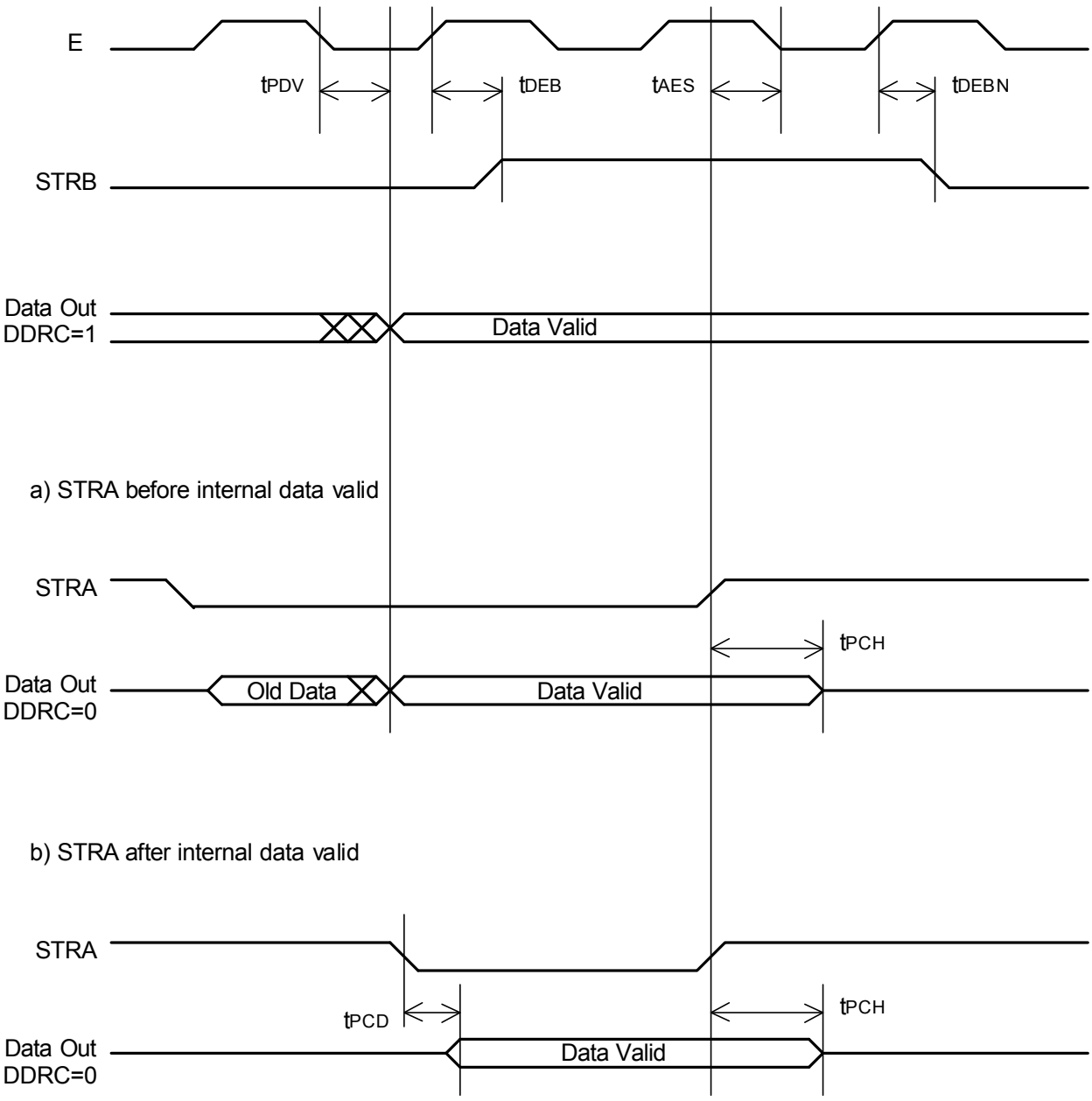


Figure 9. Port C Three-State Output Handshake Timing

Bus Timing Characteristics

(Vdd = 5.0 V ± 10%, Vss = 0 V, TA = -40°C to +85°C unless otherwise noted; see Figure 10 for detailed timing diagrams)

Ident. Number	Characteristic	Symbol	1 MHz		2.1 MHz		Unit
			Min	Max	Min	Max	
1	Cycle Time	tcyc	1000	-	476	-	ns
2	Pulse Width, E Low	PWEL	430	-	200	-	ns
3	Pulse Width, E High	PWEH	450	-	210	-	ns
4	Input and Clock Rise and Fall Time	tr, tf	-	25	-	20	ns
8	RWN Hold Time	tRWH	20	-	10	-	ns
13	Setup Time before Rising Edge of E (RWN, CSN)	tRWS	100	-	50	-	ns
15	Chip Select Hold Time (CSN)	tCSH	20	-	20	-	ns
18	Read Data Hold Time	tDHR	10	75	10	75	ns
21	Write Data Hold Time	tDHW	10	-	10	-	ns
24	Muxed Address Valid Time to AS Fall	tASL	60	-	30	-	ns
25	Muxed Address Hold Time	tAHL	40	-	20	-	ns
26	Delay Time, E Fall to AS Rise	tASD	60	-	30	-	ns
27	AS Pulse Width High	tWASH	150	-	75	-	ns
28	AS Fall to E Rise	tASED	60	-	30	-	ns
30	Peripheral Output Data Delay Time from E Rise (Read)	tDDR	20	240	10	120	ns
31	Peripheral Data Setup Time (Write)	tDSW	150	-	75	-	ns

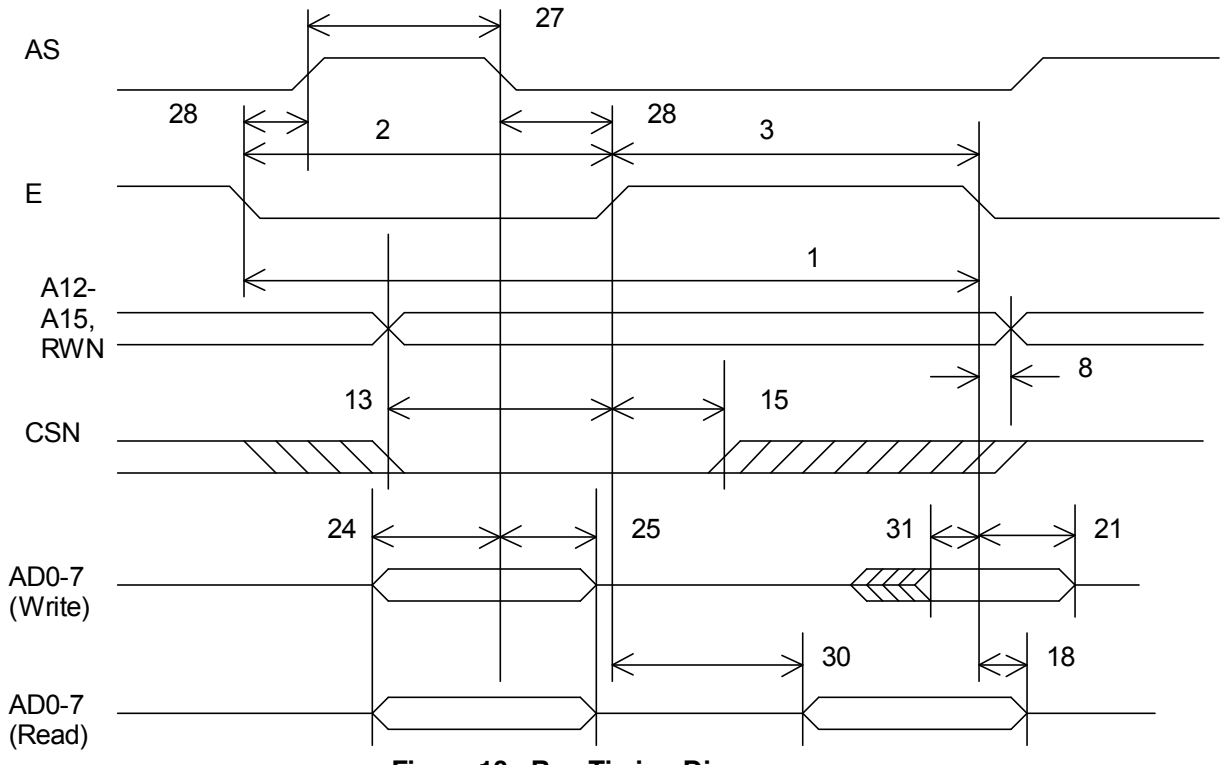


Figure 10. Bus Timing Diagram

Package Dimensions

TK68HC24FN - 44 PLCC Package

Dimension	Specification (Inches)
Package width	0.654
Width including leads	0.690
Package thickness	0.152
Lead Width	0.029
Lead spacing	0.050

TK68HC24P - 40 PDIP Package

Dimension	Specification (Inches)
Package width	0.600
Width including leads	0.610
Package length	2.050
Lead width	0.018
Lead spacing	0.100

TK68HC24 Core

This part is also available as a Verilog RTL level core. Please contact the factory for details.

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