

Features

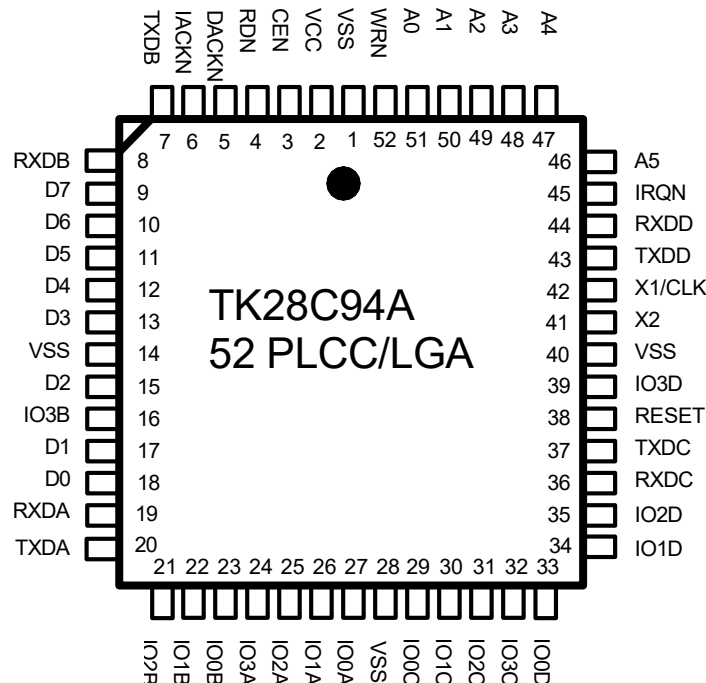
- Contains 4 industry standard UARTS.
- 8 bit transmit / receive FIFOs for each UART.
- Programmable data formats
 - 5, 6, 7 or 8 data bits.
 - Even, odd, one, zero, or no parity.
 - 1, 1.5 or 2 stop bits.
- Programmable baud rates
 - 23 fixed rates
 - user definable rates from internal counter
 - External 1X or 16X clock.
 - Separate transmit and receive baud rates.
- Parallel ports for modem status and control functions.
- 0.35u technology supports up to 3 MB operation (50 MHz clock).
- Enhanced performance
 - Digital input filter for noise suppression.
 - False start bit rejection.
 - General purpose scratch register.
 - Framing error detection and recovery.
 - Break generation and detection.
 - Overrun detection
 - Parity error detection
 - Multiple loopback modes
- Advanced interrupt controller.
 - Programmable priorities
 - Vectored interrupts
- Available in a custom 52 pin LGA that is compatible with a 52 pin PLCC footprint.
- Also available as a Verilog core for use in SOC designs.

Description

The TK28C94 is a replacement for the Philips SC28C94. It may also be used to replace the SC68C94 and the SC26C94.

The TK28C94 consists of 4 identical UARTS, organized as two groups of two. Each group contains a timer/counter which may be used for additional baud timings or for watchdog functions. Parallel ports are provided for modem control. An independent baud rate generator provides 23 different fixed baud rates. A programmable interrupt controller prioritizes all of the interrupt sources, and provides an interrupt vector for a low-overhead interrupt service routine.

Pinout



Register Address Map

Address	Read	Write	Address	Read	Write
00	Mode Reg A	Mode Reg A	1A	Reserved	Command Reg D
01	Status Reg A	Clock Sel Reg A	1B	Rx Holding Reg D	Tx Holding Reg D
02	Reserved	Command Reg A	1C	Output Port CD	Output Port CD
03	Rx Holding Reg A	Tx Holding Reg A	1D	Input Port CD	I/O Ctrl Reg C
04	Input Ch Reg AB	Aux Ctrl Reg AB	1E	Start Counter CD	I/O Ctrl Reg D
05	Int Status Reg AB	Int Mask Reg AB	1F	Stop Counter CD	Reserved
06	Cnt/Time Up AB	Cnt/Time Up AB	20	Bidding Ctrl A	Bidding Ctrl A
07	Cnt/Time Lo AB	Cnt/Time Lo AB	21	Bidding Ctrl B	Bidding Ctrl B
08	Mode Reg B	Mode Reg B	22	Bidding Ctrl C	Bidding Ctrl C
09	Status Reg B	Clock Sel Reg B	23	Bidding Ctrl D	Bidding Ctrl D
0A	Reserved	Command Reg B	24	Reserved	Power Down
0B	Rx Holding Reg B	Tx Holding Reg B	25	Reserved	Power Up
0C	Output Port AB	Output Port AB	26	Reserved	Disable DACKN
0D	Input Port AB	I/O Ctrl Reg A	27	Reserved	Enable DACKN
0E	Start Counter AB	I/O Ctrl Reg B	28	Current Int Reg	Reserved
0F	Stop Counter AB	Reserved	29	Global Int Ch Reg	Int Vector Reg
10	Mode Reg C	Mode Reg C	2A	Global Int Byte Ct	Update CIR
11	Status Reg C	Clock Sel Reg C	2B	Global Rx Hold	Global Tx Hold
12	Reserved	Command Reg C	2C	Int Ctrl Reg	Int Ctrl Reg
13	Rx Holding Reg C	Tx Holding Reg C	2D	Reserved	BRG Rate
14	Input Ch Reg CD	Aux Ctrl Reg CD	2E	Reserved	Set X1 div by 2
15	Int Status Reg CD	Int Mask Reg CD	2F	Reserved	Set X1 normal
16	Cnt/Time Up CD	Cnt/Time Up CD	30-38	Reserved	Reserved
17	Cnt/Time Lo CD	Cnt/Time Lo CD	39	Reserved	Test Mode
18	Mode Reg D	Mode Reg D	3A-3F	Reserved	Reserved
19	Status Reg D	Clock Sel Reg D			

DC Electrical Specifications (V_{dd} = 5.0 V +/- 10%, V_{ss} = 0 V, T_a = -40°C to +85°C)

Characteristics	Symbol	Min	Max	Unit
Output Voltage (I _{load} = +/- 10 uA) All Outputs All outputs except IRQN (Note 1)	V _{ol} V _{oh}	- V _{dd} - 0.1	0.1 -	V
Output Low Voltage (I _{load} = 4.0 mA)	V _{ol}	-	0.4	V
Output High Voltage (I _{load} = -0.8 mA, V _{dd} = 4.5 V) All outputs except IRQN (Note 1)	V _{oh}	V _{dd} - 0.8	-	V
Input Low Voltage All inputs	V _{il}	V _{ss}	0.8	V
Input High Voltage All inputs except X1	V _{ih}	2.0	V _{dd}	V
Input High Voltage All inputs except X1		0.8 x V _{dd}	V _{dd}	V
3-State Leakage (V _{in} = V _{ss} or V _{dd}) PC0-PC7, AD0-AD7	I _{oz}	-	+/- 1	uA
Input Current (V _{ih} = V _{dd} or V _{ss}) E, AS, R/WN, CSN, MODE, A12-A15, STRA	I _{in}	-	+/- 1	uA
Total Supply Current (Note 2)	I _{dd}	-	35	mA
Power Down Mode	I _{ddpd}	-	2	mA

Note 1. IRQN is an open-drain output. V_{oh} does not apply.

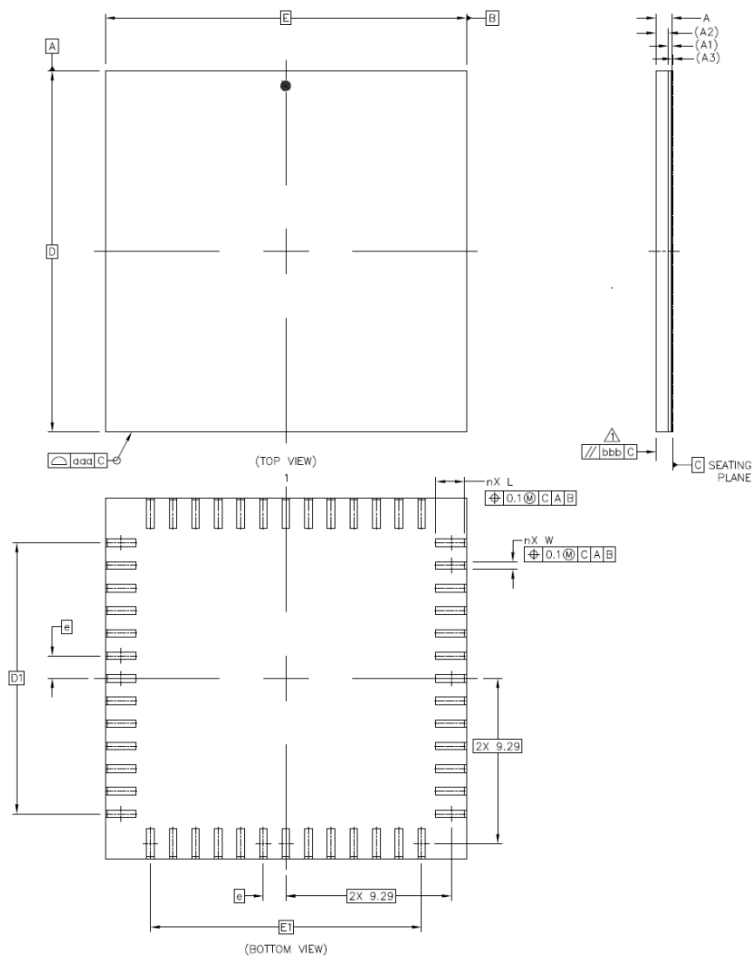
Note 2. CMOS input levels, 25°C, X1 = 4 MHz.

Ordering Information

Temperature	Reference Number	Ordering Number	Package	Lead Finish
-40°C to +85°C	TK28C94A1A	TK7954L	LGA52	RoHS

Note: The original PLCC52 package has gone obsolete. Tekmos has designed a custom LGA52 package that is compatible with a PLCC52 footprint on a PCB. The LGA52 is a drop-in replacement for the PLCC52 package.

Package Outline Drawing – LGA52



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	---	---	1
SUBSTRATE THICKNESS	A1		0.196	REF
MOLD THICKNESS	A2		0.7	REF
BODY SIZE	D		20.3	BSC
	E		20.3	BSC
LEAD WIDTH	W	0.38	0.43	0.48
LEAD LENGTH	L	1.55	1.6	1.65
LEAD PITCH	e		1.27	BSC
LEAD COUNT	n		52	
EDGE LEAD CENTER TO CENTER	D1		15.24	BSC
	E1		15.24	BSC
BODY CENTER TO CONTACT LEAD	SD		---	BSC
	SE		---	BSC
PRE-SOLDER	A3	0.01	0.05	0.09
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		---	

Contact Information

Please contact orders@tekmos.com for further information.

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Revision History

Date	Revision	Description
11/08/2019	1.04	Initial Release
06/11/2025	1.05	Added Ordering Table, Contact Information & Revision Table
04/21/2026	1.06	Updated ordering table to add TK7954L, added verbiage about the LGA52 package replacing the PLCC52. Added LGA52 Package Outline Drawing

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