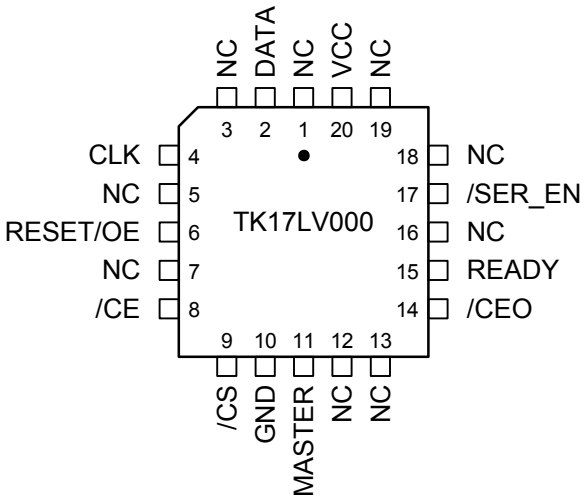
TK17LV000 Series of Serial Configuration Memories

DS002 (v1.0) November 8, 2019 Preliminary Product Specification

Features

- 512 Kb, 1 Mb, 2Mb, 4 Mb, and 8 Mb Serial Configuration Memories (SCM)
- Direct replacement for Atmel ® AT17LV000 and AT17LV000A series memories
- All memory sizes use the space saving, 20 pin PLCC package
- Stores configuration data for Xilinx ®, Orca ®, Altera ® and Atmel ® FPGAs
- Up to 30 MHz clock reduces FPGA configuration time by 250%
- 3.3V operation for compatibility with the newer FPGAs
- In-system reprogramability for field upgrades and engineering development
- 0.32u CMOS flash technology, with over 1,000,000 write cycles and a 20 year data retention
- Cascadable design supports the largest FPGA bitstream requirements
- Programmable reset polarity supports different system architectures
- READY Pin, with programmable digital delay insures reliable power-up
- Low-power standby mode

Pin Out



General Description

The TK17LV000 series of serial configuration memories provide an easy-to-use, cost-effective configuration memory for FPGAs. Capable of a 30 MHz data load rate, the TK17LV000 series provides a new level of support for large FPGAs, while retaining backwards compatibility with existing smaller configuration memories and PC board layouts.

The TK17LV000 series supports serial loading for most Xilinx ®, Atmel ®, Altera ® and Lucent/Agere ® FPGAs. Multiple FPGAs in series may be configured by a single TK17LV000 series part. Large FPGAs needing in excess of 8 Mb may be supported by cascading multiple TK17LV000 series parts. Conversely, existing 2 Mb or smaller parts, in stand-alone or cascade mode, can be replaced by the TL17LV000 series without modifying the existing circuit board. And the high speed capability reduces the FPGA configuration time for advanced FPGAs.

The TK17LV000 series supports a number of user programmable options. The user may set the polarity on the RESET / OE pin. The user may also program the power-on-reset delay for the READY signal, which signifies the presence of a valid power level.

The choice of which chip enable input to use is user programmable, allowing the TK17LV000 to be compatible with existing applications using the Atmel ® “A” series. The TK17LV000 also supports both the sourcing of the DCLK clock signal and control of the DCLK frequency.

The TK17LV000 series incorporates a sophisticated approach to In-System Programming that supports multiple cascaded devices while eliminating the need for external support circuitry.

The TK17LV000 series can be programmed in system by software, out of the system using industry standard programmers, or purchased pre-programmed by the factory.

Pin Descriptions

Table 1 - Pins and descriptions

Pin	Name	Type	Description
2	DATA	I/O	Three-state output for FPGA mode, open-drain for serial mode.
4	CLK	I/O	Clock input. Can be programmed to be the DCLK output for Altera ® support.
6	RESET/OE	I	Reset / Output Enable when in FPGA mode. User programmable as either /RESET - OE or RESET - /OE. Pin is unused in the serial mode.
8	/CE	I, pull-up	Chip Enable input
9	/CS	I, pull-up	Chip Select input. Used in existing “A” series applications.
10	GND	S	Ground pin
11	MASTER	I, pull-up	Identifies first chip in a cascaded mode. Only used in conjunction with the In-System Programming of cascaded memories. Not used during FPGA configuration.
14	/CEO	O	Enables downstream cascaded memories.
15	READY	O, pull-up	Open-drain device ready signal. Driven low during power-on-reset and during serial mode. Length of reset delay is programmable.
17	/SER_EN	I, pull-up	Mode select. 1 = FPGA configuration, 0 = serial mode
20	VDD	S	+3.3 V power supply pin

Detailed Pin Descriptions

The TK17 series of serial configuration memories operate in one of two modes: FPGA mode and Serial mode. The function of most pins depends on the operating mode.

DATA

Serial Mode. The DATA pin is an open-drain output with a dynamic precharge. An external pull-up resistor is required if the serial mode is used.

FPGA Mode. The data pin is a three-state output in the FPGA mode. The data pin is enabled when CE_N (or CS_N) is low, RESET_OE is active OE, and the chip is not yet finished with transferring its data. Once the chip is done, the DATA pin will remain in a high impedance mode until the chip has been reset.

CLK

Serial Mode. This is the clock for the serial bus.

FPGA Mode. If the part is programmed as a master in Altera ® mode, the CLK pin will be an output, providing the DCLK signal. In all other configurations, the CLK pin is an input.

Attempting to read the part prior to the completion of the initialization sequence will result in all ones being read on the data bus.

In using the DCLK option, the speed of the DCLK signal may be set during programming. DCLK becomes a divide-by-N (2<N<255) from the internal 120 MHz clock, with a 50% duty cycle.

RESET_OE

Serial Mode. RESET / OE is not used in the Serial mode.

FPGA Mode. The RESET / OE pin either resets the address counter, or provides an output enable for the DATA pin.

The user may program the polarity of this pin to match the system requirements.

/CE and /CS

These pins are identical in function. The choice of which pin to use is set as a programming option. The unused pin should be left unconnected. Atmel ® “A” series applications use /CS (pin 9) as the chip enable input. Most other applications use the /CE (pin 8).

Serial Mode. The chip enable function is used during the In-System Programming of cascaded memories. The chip enable has no effect if the MASTER pin is high.

FPGA Mode. The chip enable must be low, along with an active output enable, for the FPGA configuration to begin.

If the chip has been programmed as a slave device, and if pipelining is enabled, the external chip enable signal is delayed internally by one clock before it is used in the chip state machine.

MASTER

Serial Mode. The master pin is tied low on slave devices in those cases where the user intends to perform In-System Programming on cascaded memories. It is left high on the master device, and may be left unconnected if this function is not being used.

When MASTER is low, chip enable must be active for the chip to respond to programming commands.

FPGA Mode. This pin is not used, and may be left unconnected.

/CEO

Serial Mode. This pin is used to enable downstream memories in those applications requiring cascaded In-System Programming.

FPGA Mode. This pin goes active after the last data bit has been read, providing that chip enable is also active.

If the pipelining option has been set, then this pin goes active on the next to last bit being read.

READY

Serial Mode. This pin is always low during Serial Mode.

FPGA Mode. This pin is pulled low during chip initialization, and remains low until the chip is ready to be read.

The user may program an additional delay, from 1 ms to 255 ms, to allow the system power supplies to stabilize before beginning the FPGA configuration.

SER_EN

Serial Mode. Bringing this pin low resets the chip and puts it into the Serial Mode. Bring SER_EN low also forces the READY output low.

FPGA Mode. The chip is in the FPGA mode when this pin is high. Bringing it from low to high triggers a chip power-on initialization cycle. This allows the results of In-System Programming to take effect without having to power the system down.

Altera ® applications use pin 18 as the SER_EN input, while leaving pin 17 as a No-Connect. In those Altera applications that do not utilize In-System Programming, the SER_EN pin may be left floating.

Memory Sizes

The TK17 series contains 5 family members. Note that the TK17LV040 and the TK17LV080 reserve 16 bytes for internal use.

Part Number	Memory Size
TK17LV512	524,288 x 1
TK17LV010	1,048,576 x 1
TK17LV020	2,097,152 x 1
TK17LV040	4,194,176 x 1
TK17LV080	8,388,480 x 1

Unconnected Pins

The /CS, /CE, /SER_EN, and MASTER pins have internal pull-up resistors to pull the pin to a valid logic level when the TK17LV000 series part is being used to replace an existing part.

The DATA pin, and in some applications, the CLK pin require an external pullup, and should not be allowed to float.

Typical FPGA Application

Figure 2 shows a simplified schematic showing two TK17LV080s cascaded to provide 16 Mb of configuration memory. The schematic also shows how In-System Programmability can be provided without the need for external switching devices.

The CLK pins are wired in parallel and connected to the FPGA's CCLK pin.

The DATA pins are wired in parallel and connected to the FPGA's DIN pin.

The RESET/OE pins are wired in parallel and connected to the FPGA's INIT pin. The TK17LV080s should have the RESET/OE polarity programmed to be active-low.

The CE pin of the lead device is connected to the DONE pin of the FPGA. The CEO of the lead device is connected to the downstream device's CE input.

The MASTER pin of the downstream device is tied to ground.

The READY pins are tied together and to the FPGA's reset pin.

Both /SER_EN pins are tied together.

Using the TK17 Series with FPGAs

The TK17LV000 series can be used to configure the following low voltage FPGAs. Please reference the individual application notes for connection details.

Manufacturer	Series
Lucent / Agere	Orca 2T ®
Lucent / Agere	Orca 3T ®
Lucent / Agere	Orca 4 ®
Altera	Flex 10K ®
Altera	Apex 20K ®
Atmel	AT6000 LV ®
Atmel	AT40K LV ®
Xilinx	XC4000 ®
Xilinx	Spartan XL®
Xilinx	Spartan II ®
Xilinx	Virtex ®
Xilinx	Virtex E ®
Xilinx	Virtex II ®

Standby Mode

The TK17LV000 will enter a low-power standby mode whenever /CE (or /CS) is high.

The power will be further reduced after configuration is complete and the clock has stopped. At that time, the supply current becomes composed of internal leakages and the currents drawn by any pullup resistors that are tied low.

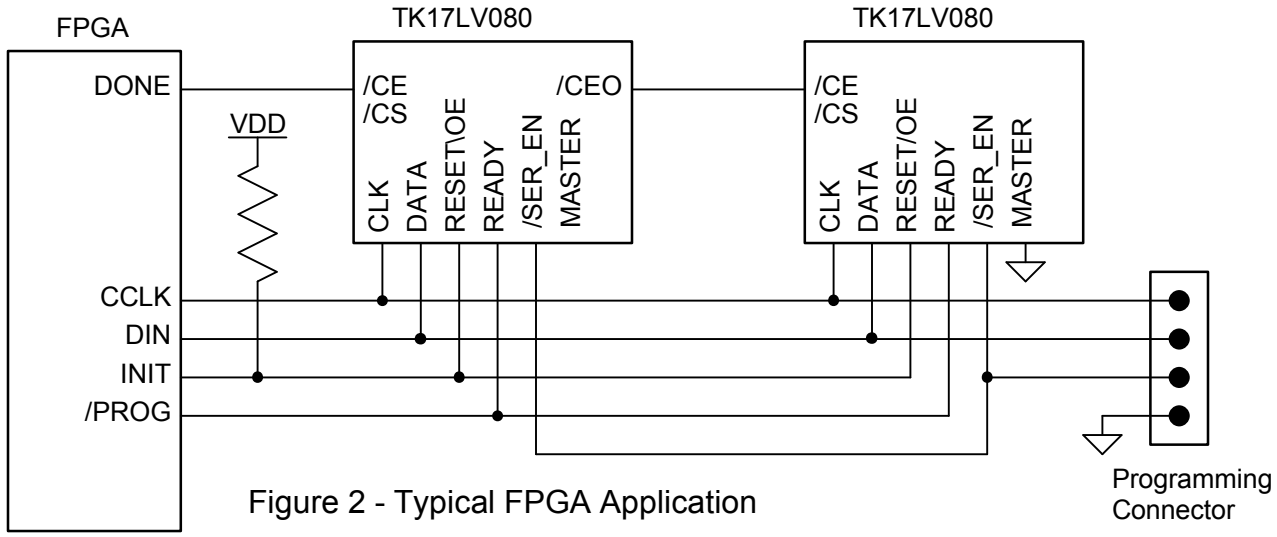


Figure 2 - Typical FPGA Application

Programming the TK17LV000

The TK17LV000 is capable of being programmed when /SER_EN is low. The TK17LV000 is programmed through the use of normal supply voltages, making it ideal for those applications requiring In-System Programming.

The TK17LV000 may be programmed out-of-system using industry standard programmers, in-system using Tekmos supplied (or user developed) software, or they may be programmed by the factory.

Detailed programming instructions are provided in the programming application note.

User Programmable Features

The TK17LV000 series provide a number of user-selectable options that minimize external component count and improve overall system performance.

RESET/OE Polarity

The polarity of the RESET/OE pin may be programmed.

Pipelined Chip Enable

The /CE (or /CS) and /CEO functions may be pipelined. This improves the CLK to Out performance of the DATA pin when cascaded devices are switching from one device to a downstream device.

Chip Enable Source

Either the /CE or /CS pin may be selected as the source of the chip enable function.

Power-On-Reset Delay

The width of the READY low time may be extended from 1ms to 255 ms. This provides extra time to allow other supplies to stabilize in a multi-supply system.

DCLK mode

This enables the TK17LV00 series to provide the clock signal when used with an FPGA series that requires an external clock.

The speed of the supplied DCLK signal is also programmable as a divide-by-N (4<N<255) from an internal 120 MHz oscillator.

Electrical Specifications

Maximum Ratings

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	Vdd	-0.5	4.0	V
Input Voltage	Vin	Vss – 0.3	Vdd + 0.3	V
Current Drain per Pin	Imax		25	mA
Operating Temperature Range	Ta	0	70	^{o}C
Storage Temperature range	Tstg	-55	+150	^{o}C

DC Electrical Specifications (Vdd = 3.3 V +/- 10%, Vss = 0 V, Ta = 0^{o}C to +70^{o}C)

Characteristics	Symbol	Min	Max	Unit
Input high level	V_{IH}	2.0	Vdd	V
Input low level	V_{IL}	0.0	0.8	V
Output high level @ Ioh = 8 mA	V_{OH}	2.4	Vdd	V
Output low level @Iol = 8 mA	V_{OL}	0	0.4	V
Supply current, Active mode, CLK = 10 MHz	I_{CCA}		20	mA
Input or Output Leakage current	I_{L}	-10	10	uA
Supply current, standby mode	I_{CCS}		10	uA

AC Electrical Specifications (Vdd = 3.3 V +/- 10%, Vss = 0 V, Ta = 0°C to +70°C)

Characteristics	Symbol	Min	Max	Unit
/OE to Data Delay	T_{OE}		15	ns
/CE to Data Delay	T_{CE}		15	ns
CLK to Data Delay	T_{CAC}		15	ns
Data Hold From /CE, /OE, or CLK	T_{OH}	0		ns
/CE or /OE to Data Float Delay	T_{DF}		15	ns
CLK Low Time	T_{LC}	12		ns
CLK High Time	T_{HC}	12		ns
/CE Setup Time to CLK	T_{SCE}	8		ns
/CE Hold Time from CLK	T_{HCE}	0		ns
/OE High Time	T_{HOE}	25		ns
Maximum Input Clock Frequency	F_{MAX}	30		MHz
CLK to Data Float Delay	T_{CDF}	10		ns
CLK to /CEO delay	T_{OCK}	15		ns
/CE to /CEO Delay	T_{OCE}	15		ns
Reset /OE to /CEO delay	T_{OOE}	15		ns

Notes:
1. AC measurements made with a 50 pF load, at a 50% supply voltage level.
2. Float delay measured with a 3.3K resistor tied to opposite supply, measured after a +/- 0.2V change in voltage level.

Timing Diagrams

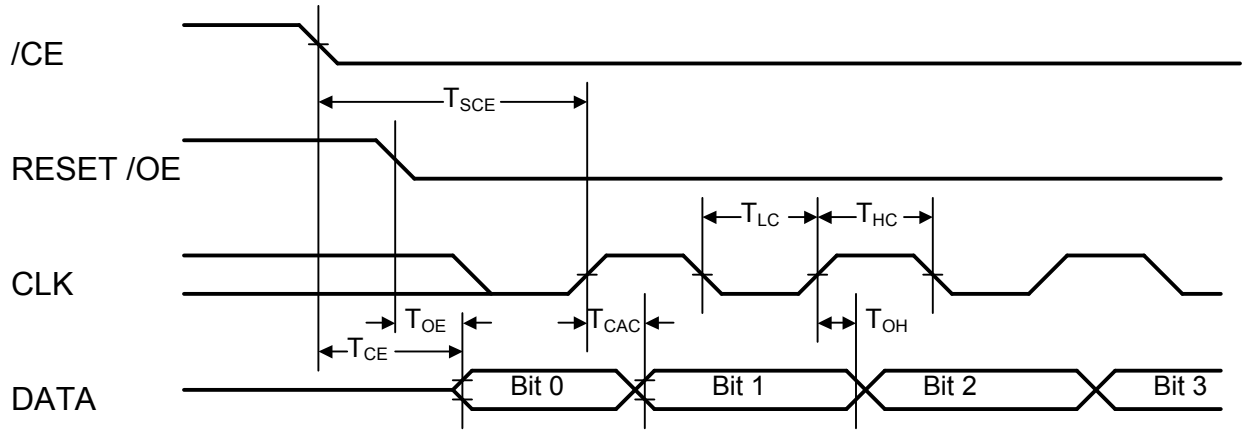


Figure 3 - Startup Waveforms

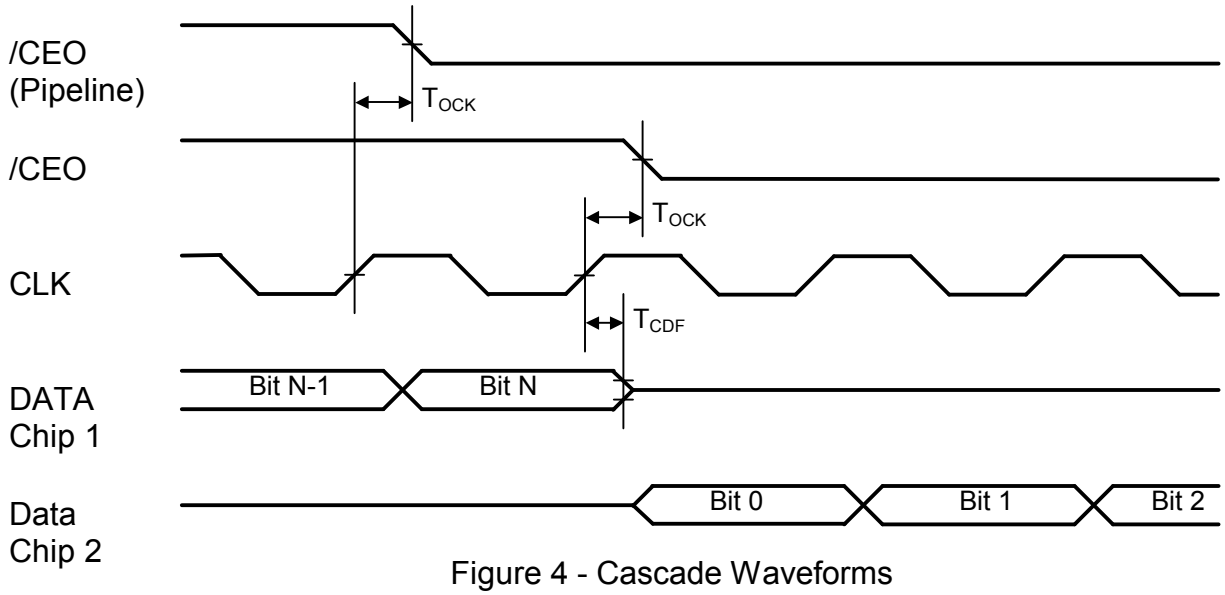


Figure 4 - Cascade Waveforms

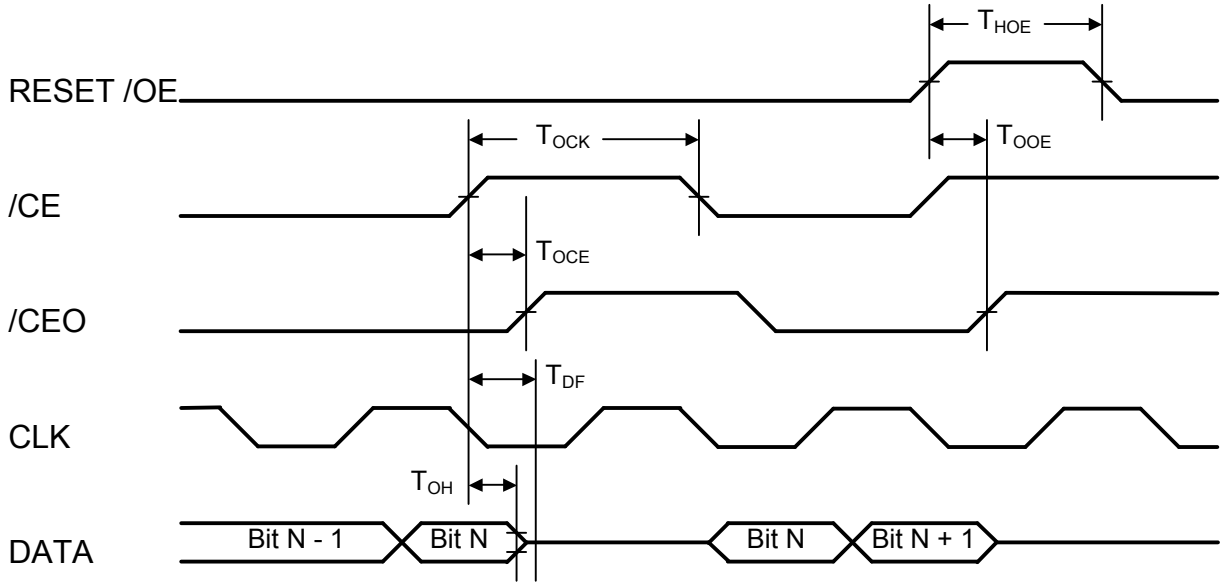
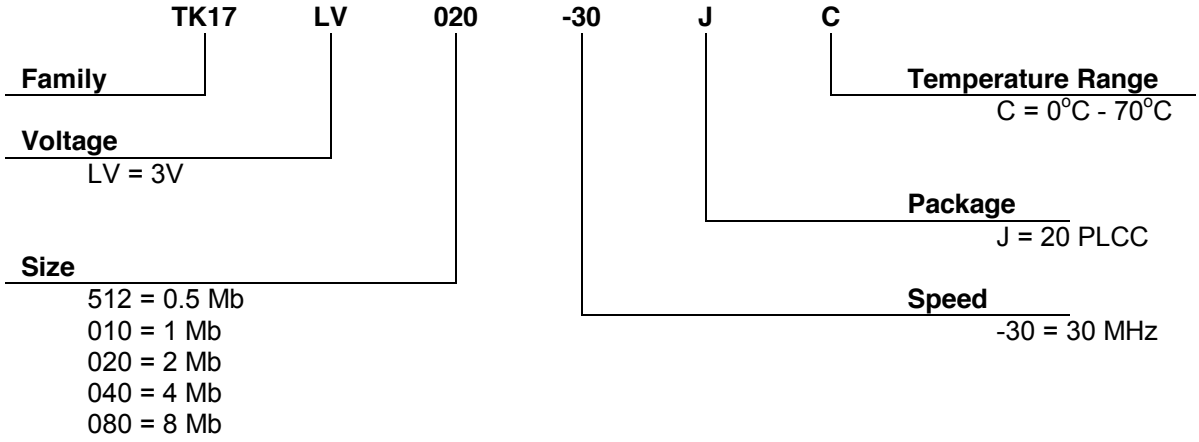


Figure 5 - End Waveforms

Ordering Information

Here is the explanation for the TK17LV000 series ordering codes.



Contact Information

The TK17LV000 series may be ordered directly from Tekmos

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Revision History

Date	Revision	Description
8/20/01	1.0	Initial release