TEKMOS

High Temperature ASICs 250C and 200C

November 8, 2019 Data Sheet

SOI ASIC Features

- 250C operation.
- Supports designs up to 30K gates with 1.0u technology.
- SOI (Silicon-On-Insulator) process for diode leakage and SCR control.
- Tungsten interconnect for metal migration control.
- Small lot size option with MLM masks to reduce production costs.
- Ceramic Packaging or die
- Aluminum Bonding for Reliability
- RAM, ROM and 8-bit ADC cells available

Bulk Silicon Features

- 200C operation in ceramic, 150C in plastic.
- Supports up to 500K gates with 0.35u technology.
- Gate array technology minimizes NRE costs.
- EEPROM available with extended data retention.

All Tekmos ASICs

- Flexible pinout to match existing devices.
- Supports multiple package types.
- Easy engineering interface. We work from your existing files.
- Small or large production quantities supported.
- Guaranteed to work – no risk
- Fast turnaround on most FPGA replacements
- Merged design technology.

Mixed Signal

- Process supports resistors and capacitors.
- Cells include Op-Amps, Voltage References, A/D and D/A converters

High Temperature Limits

Most ASICs are sold at an industrial temperature grade of 85C. Performance to the military limits of 125C is also available. But what about higher temperatures?

The ability to operate at higher temperatures is limited by design issues, packaging issues, reliability issues, and basic silicon properties. The standard XA35 technology can be extended up to 200C. The Tekmos SOI technology, with Tungsten interconnects, can be extended all the way to 250C.

Diode Leakage

Silicon transistors contain parasitic reverse-biased diodes on all junctions. The diode leakage current increases with temperature, and eventually reaches a point where it prevents correct circuit operation. Diode leakage is the main factor in limiting our XA35 process technology from operating any higher than ~225C. The diode leakage currents also aggravate the metal migration reliability problem.

The Tekmos SOI process is based on an SOI (Silicon-On-Insulator) technology. In an SOI process, diode junctions are eliminated, except for the extremely small vertical interface between the diffusion and the transistor channel. In a typical

case, the area of the diode junction is reduced by a factor of 15. And that allows us to achieve 250C operation.

Metal Migration

High current flow in aluminum interconnect can create voids that will eventually lead to opens. The rate of voiding is a function of temperature, and poses a serious reliability problem for high temperature operation. The Tekmos SOI process makes use of an optional Tungsten metallization process that minimizes the migration effect.

Tungsten is roughly 4 times more resistive than Aluminum, and so this must be compensated for in the circuit layout. The use of Tungsten is key for achieving reasonable reliability at 250C.

Hot Electron Injection

Threshold shifts due to hot electron injection are a well-known phenomenon that gets worse with increasing temperature. Tekmos has developed special monitors that check for hot electron bias shifts, and we use that information to predict the maximum operating life of a product.

Assembly

The gold aluminum interface is prone to corrosion problems at high temperature. One solution is to use aluminum bonding. A second option is to have the bond pads gold plated prior to assembly. Tekmos also offers a dual bond pad approach to prevent probe marks on the pads from affecting the bond reliability.

Merged Designs

Tekmos can merge multiple designs into a single die. This allows for a reduction in the total NRE, and supports products whose normal volume would not justify a stand-alone ASIC.

Tekmos ASIC Implementation

With the experience of hundreds of ASICs behind us, we have simplified the ASIC procedure.

Design Interface

ASIC implementation begins with your design. We can start wherever is most convenient for you. That can be an RTL description, a design currently in an FPGA, or design files from an existing ASIC.

Once we have your files, we will convert them into our internal library, and verify the correct operation through simulation.

Simulations and Sign-Off

Original simulations (if they exist) will be enhanced with Tekmos generated simulations and used for production testing.

Replacing an FPGA or existing ASIC means that Tekmos is responsible for the post-route signoff. Customer participation, while optional, is encouraged.

Prototypes and Production

The design will be fabricated, assembled, and tested. Prototypes are available in about 8 to 12 weeks after tape-out. Production can begin after prototype approval.

Volume Requirements

Many high temperature ASICs have minimal volume requirements. To support this, Tekmos ASICs can be configured as engineering runs, which are one-time efforts that can produce exactly the number of required parts.

Packaging

Plastic packages work well with temperatures of 150C or below. Tekmos supports a full line of plastic packages for any application.

Temperatures above 150C generally require ceramic packages. The most common ceramic packages are DIPs and PGA type packages. Lead times vary with package type.

Schedules

The design phase typically takes from 2 to 4 weeks. Prototyping varies with the process, but typically takes from 8 to 12 weeks.

Additional Services

Tekmos supports additional back end services such as full temperature testing and burn-in. Contact the factory for details.

Quotations

ASICs

The size of a given design can vary considerably, depending on the number of gates, the amount of memory, and the number of used pins. On the other hand, the cost of the ASIC replacement is directly linked to the design size. That is why we need to review the design netlist to provide an exact quotation.

FPGAs

Tekmos can provide a budgetary quotation based on the full FPGA part number and desired annual volume. A more accurate budgetary quotation can be obtained if the FPGA utilization report is provided.

Standard Products

Any of the Tekmos microcontrollers can be available in a high-temperature version. Other circuits may be available depending on their complexity. We can prepare a quotation from a data sheet.

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Revision History

Date	Revision	Description
10/30/09	1.0	Initial release
4/18/2014	1.1	Update SOI Information