TEKMOS

High Temperature Mixed Signal Capabilities

November 8, 2019 | Product Overview

Features

- Up to 300°C Operation
- Will support most analog functions.
- Easily combined with up to 30K digital gates.
- 1.0u SOI Process, with double poly and triple metal.
- Tungsten Interconnect
- Gold pads available
- 3.3 or 5 volt operation.
- Available in DIP, SO, or PGA ceramic packages.
- Ideal for down-hole oil applications or jet engine controls.

General Description

High temperature electronics operate in one of the most demanding electronic environment. Junction leakage doubles with every 10°C increase in temperature. For bulk silicon devices, the leakage becomes significant above 175°C, and intolerable above 225°C. And while digital logic can withstand some leakage, most analog circuits cannot.

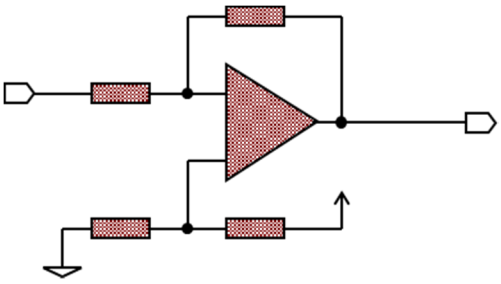
Leakage is a problem that cannot be overcome with clever design tricks. It requires a different process. And that process is SOI (Silicon On Insulator).

In this process, oxygen is implanted beneath the devices. And the field oxide extends down to the implanted oxide layer, providing external isolation. Then, the diffusions are deep enough so that they too touch the buried oxide. This eliminates the bottom and sidewall junctions. And without a junction, there can be no junction leakage.

There is a small junction between the source / drain diffusions and the transistor channel. So while the junctions have not been totally eliminated, that have been reduced in area by a factor of 1,000. And that gives the SOI process an additional 100°C of operation.

As with all engineering choices, there are tradeoffs. On the positive side, stray capacitance has been eliminated, along with the voltage dependency of diffused resistors. And with most wells tied to the transistor sources, the body effect has been eliminated.

On the negative side, layout density is decreased, and overall layout is more difficult. There are no vertical bipolar devices, just lateral ones. We do not have an EEPROM cell, so trimming becomes more complicated. And the 1u technology limits the circuit size.



Applications

To start with, anything that can be done in bulk silicon can also be done in the SOI process.

In the down-hole environment, there is demand for instrumentation amps, ADCs, DACs, and the occasional op-amp. All of these are easily made, and because of the lack of junctions, will have better performance than achieved with bulk devices.

Many down-hole measurements are made on low frequency signals, allowing Sigma-Delta ADCs to be used with up to 24-bit accuracy.

And since the SOI devices are totally isolated from the substrate, the analog supplies can be +/- 2.5v volts, and still work with a digital section operating from a 5 volt supply.

Technical Interface

Tekmos provides multiple approaches for an analog technical interface. Our customers are free to choose the one that best suits their need.

Tekmos Design to Specification

Tekmos will design the analog functions to meet a customer specification. We will be responsible for all aspects of the analog development, including design, layout, and test development. Ultimately, Tekmos is responsible for the satisfactory performance of the design within the customer system.

Tekmos will conduct an initial design review with the customer to review their system requirements, and to establish the design specifications.

Our customer may review the design at any point, and can optionally participate in any internal design reviews.

When the design is complete, Tekmos will publish a data sheet that documents the design and sets forth the performance specifications.

Customer Design, Tekmos Layout

For those customers who would rather design the circuit themselves, Tekmos can provide spice models and available device sizes to customers. This allows the customer to exercise total control over the design of their circuit.

Tekmos will perform a manual layout of the design, and feedback extracted capacitance information for approval.

Tekmos will also review the design for compliance with the agreed to specifications and for testability.

Full Customer Design Cycle

Tekmos can accept GDS layouts of customer designs on our analog arrays for those customers wishing to exercise the ultimate in design control.

Tekmos will run DRC and LVS checks on the supplied database to insure conformance to wafer fabrication requirements. As is our policy with any customer submitted design, Tekmos will review the design for compliance with the agreed to specifications and for testability.

Tekmos can also accept all layer GDS databases, though that entails a standard-cell flow, which has other economic and scheduling ramifications.

Detailed Array Description

Tekmos uses an analog tile approach for its analog design and layout. The main tile contains the components for an op-amp, along with capacitors that can be used in a number of ways, including switched capacitor designs. The tiles also contain a number of general purpose resistors.

We have specialty tiles for special functions, such as bandgap voltage references and charge pumps.

The digital logic portions of the mixed signal device are implemented as a gate array. We will add as many gates as required, taking into account the anticipated utilization.

This approach allows us to start wafers before the design is completed. This can cut 5-7 weeks off of the overall development schedule.

Manufacturing Considerations

NRE Charges

Depending on the characteristics of the circuit, there may be an additional NRE charge for analog design. This covers the additional engineering time to design, simulate, and layout the circuit.

The presence of analog circuitry has no effect on the mask or fabrication charges.

Testing

Many analog functions can be satisfactorily tested using standard digital testers. This is particularly true in those cases where test modes have been added to the analog circuitry. If this is the case, then the presence of mixed-signal circuitry will not affect the manufacturing prices.

Some analog circuits may require either special testing hardware, or the use of special analog testers. These requirements can affect the NRE or the production costs, or both.

Manufacturing Order Size

Tekmos has several programs designed to reduce the fab NRE charges and the manufacturing costs at low volumes. We can usually incorporate mixed signal designs within these programs.

Analog Trimming

The Tekmos arrays do not support analog trimming. Such activities are not compatible with a low cost gate array technology flow.

A limited trim capability can be provided by using bond options to adjust resistor ratios.

The layout can be implemented in a manner so that adjustments can be made using a single metal mask. This minimizes the cost of adjustments.

Packaging and Pin-Out

The Tekmos arrays can be packaged in virtually any commercially available package. This includes PLCC packages from 28 pins up to 84 pins, PQFP packages from 80 to 240 pins, TQFP packages from 44 to 144 pins, QFN packages from 6 to 68 pins, and BGA packages in any ball count.

The analog requirements may constrain the pinout of the analog signals and supplies to pins that are physically close to the internal analog components.

There are no constraints on the I/O pad sites themselves. Each site may be programmed to be a supply, a digital signal, or an analog signal.

The power ring may also be partitioned to support independent or multiple supplies for use with the analog components.

Case Studies

Here are several examples of mixed signal circuits implemented on Tekmos arrays.

Voltage Reference

The application was to provide a reference voltage for an interface to single-ended ECL signals.

The design was built around a band-gap voltage reference, which creates a 1.2V output, referenced to Vss.

The system required a 3.65 volt reference, but since ECL signals use a positive ground, the reference voltage must track Vdd. We accomplished this by using a current mirror to both scale the band-gap voltage and to change the reference to Vdd.

This new reference was then supplied to all ECL inputs. Each individual ECL input made use of the built in comparator at each pad site to compare the ECL input with the ECL reference.

We were concerned that the offset of the comparators might affect system performance. So, we provided a means for adjusting the reference voltage +/- 20 mV through the use of bond options. Such an adjustment would not require additional mask costs.

Duty Cycle Adjuster

We needed a circuit that would restore the duty cycle of a recovered input clock to 50%. We did not want to use a PLL / Divide-by-2 approach because of the high clock speed, and because of a concern over the jitter introduced by a PLL.

Instead, we created a new clock by using an RS latch that was set by the leading edge of the clock, and reset by the same edge after passing through a voltage controlled delay line. The delay line was constructed out of inverters whose speed was set by a control voltage.

We used an on-chip RC filter to detect the duty cycle of the generated clock. The filter was built out of series poly resistors, and every capacitor that was not used as compensation in the op-amps.

The DC output voltage is proportional to the duty cycle of the generated clock. This voltage was compared to a Vdd/2 reference by an op-amp, which produced an error signal that controlled the delay line.

Analog PLL

The application required generating a 3X internal clock off of a 16 MHz reference. The VCO was set to a nominal 100 MHz frequency with a divide by 2 on the output, and was built out of internal gate transistors to achieve the desired operating speed.

The 2nd-order loop filter was on-chip, and constructed out of the resistors and capacitors contained in the corner analog array. Separate supplies were used to reduce digital noise.

High Temperature ADC

The application called for an 8-bit ADC, with an operating temperature of 275C. In an unusual variation, we used N+ resistors instead of poly resistors to make the DAC. N+ resistors have much better matching characteristics than poly. However, they are not normally used for DACs because of a voltage coefficient caused by the junctions. Since the SOI process does not have junctions, we could use the N+ resistors.

The ADC was functional up to 320C. However, the accuracy began to degrade at 300C, and was only about 4-bits accurate at 320C. This was to be expected, since even with SOI, there remain small junctions at the channel edge.

Contact Information

Tekmos, Inc.
7901 E Riverside Rd.
Bldg. 2, Suite 150
Austin, TX 78744
512 342-9871 phone

Sales@Tekmos.Com
www.Tekmos.com

Revision History

Date	Revision	Description
6/29/17	1.0	Initial Release