TEKMOS

Preliminary
TK80H51
250C Microcontroller

November 8, 2019 | Product Overview

Features

- 250C Operation
- Optional Expanded Address Bus **NEW**
- Bootstrap Operation Out of RAM **NEW**
- 8 Bit Microcomputer with 8051 Architecture
- 512 Bytes Internal RAM
- 8K Internal ROM
- 8-channel, 8-bit ADC **NEW**
- SPI Port **NEW**
- Low Standby Current At Full Supply Voltage
- 0-16 MHz Operation (12 clock mode)
- 7 8-Bit Bidirectional Ports **NEW**
- 8051 Family Peripherals
- Multiple Package Options
    - 40 pin CDIP
    - 68 pin PGA
    - Die
- Three 16 bit timer/counters
- Full Duplex Serial Channel With Hardware Address Decode
- Multiple Source, Four Level Interrupt Priority Capability
- Programmable Counter Array
- Watchdog Timer For Greater System Reliability
- Dual Data Pointers

General Description

The TK80H51 family, based on the 8051 architecture, is designed to work in high temperature environments up to 250C. The E (Enhanced) version of the TK80H51 provides a non-multiplexed address and data bus, the 8-bit ADC, three additional parallel ports, and the SPI port.

The enhanced version also supports a RAM-based bootstrap mode, allowing for the downloading of RAM based programs into an existing system. In the bootstrap mode, the 256 bytes of XRAM are re-mapped from the data space into the program space. The ROM-based bootstrap program receives 256 bytes serially, and stores them in the RAM. After the user program has been received, the bootstrap program jumps to the RAM for further operation.

The TK80H51 family is made on an SOI process, using tungsten interconnect. This technology is what allows the TK80H51 to operate at 250C operation.

In the TK83H51 series, the internal 8K masked ROM provides a permanent program storage that will not degrade with temperature. As with all 8051 family members, the internal storage can be augmented with external program storage.

The TK80H51 family contains seven 8 bit bidirectional parallel ports, two external interrupt sources, three timer/counters, a serial port with a hardware interrupt capability and a frame error detect flag, power management, a programmable counter array (PCA), an 8-bit, 8-chanel ADC, and a SPI port. These peripherals are supported by a multiple source, four level interrupt capability. The core processor contains 256 bytes of scratchpad RAM and another 256 bits of XRAM that can be used as program storage.

Family Summary

The TK80H51 family members mainly differ by the amount of embedded memory, and whether the package has enough pins to support the new embedded peripherals.

Part	ROM	RAM	PKG	Available
TK80H51	0 KB	512	40	2014 Q4
TK80H51E	0 KB	512	68	2014 Q4
TK83H51	8 KB	512	40	2014 Q4
TK83H51E	8 KB	512	68	2014 Q4

Contact Information

The TK80H51 family series may be ordered directly from Tekmos

512-342-9871 phone
Sales@Tekmos.com
www.Tekmos.com

Revision History

Date	Revision	Description
5/01/14	0.1	Internal Review