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1. Description

Based on the TK80C51, the TK83C749 is economically priced and comes in a small package size. Tekmos uses high-density CMOS technology to construct the TK8XC749 Microcontroller, decreasing CMOS latch-up sensitivity through epitaxial substrate.

The programmed selection and masked ROM TK83C749 operate identically to each other; therefore, references to the TK83C749 also pertain to the TK87C749.

The TK8XC749 contains a 2k x 8 ROM, a 64 x 8 RAM, 21 I/O lines, a 16-bit auto-reload counter/timer, a fixed-priority level interrupt structure, an on-chip oscillator, a five channel multiplexed 8-bit A/D converter, and an 8-bit PWM output.

Additionally, the device comes with two power-reduction modes: idle and power down.

2. Features

- Available in erasable quartz lid or One-Time Programmable plastic packages
- TK80C51-based architecture
- Small package sizes
- 28-pin DIP
- 28-pin Shrink Small Outline Package (SSOP)
- 28-pin PLCC
- Wide oscillator frequency range: 3.5 MHz to 16 MHz
- Low power consumption:
- Normal operation: less than 11 mA @ 5 V 12 MHz
- Idle mode
- Power-down mode
- 2k x 8 ROM (TK83C749)
- 64 x 8 RAM
- 16-bit auto reloadable counter / timer
- 5-channel 8-bit A/D converter
- 8-bit PWM output / timer
- 10-bit fixed-rate timer
- Boolean processor
- Can be used with CMOS and TTL
- Ideal for logic replacement, consumer, and industrial applications

3. Part Number Selection

ROM	Temperature Range °C and Package	Frequency	Drawing Number
P83C749EBP N	0 to +70, 28-pin Plastic Dual In-line Package	3.5 to 16MHz	SOT117-2
P83C749EBA A	0 to +70, 28-pin Plastic Leaded Chip Carrier	3.5 to 16MHz	SOT261-3
P83C749EBD DB	0 to +70, 28-pin Shrink Small Outline Package	3.5 to 16MHz	SOT341-1

Table 1: Part ROM, Temperature Range, Frequency, and Drawing Number

4. Block Diagram

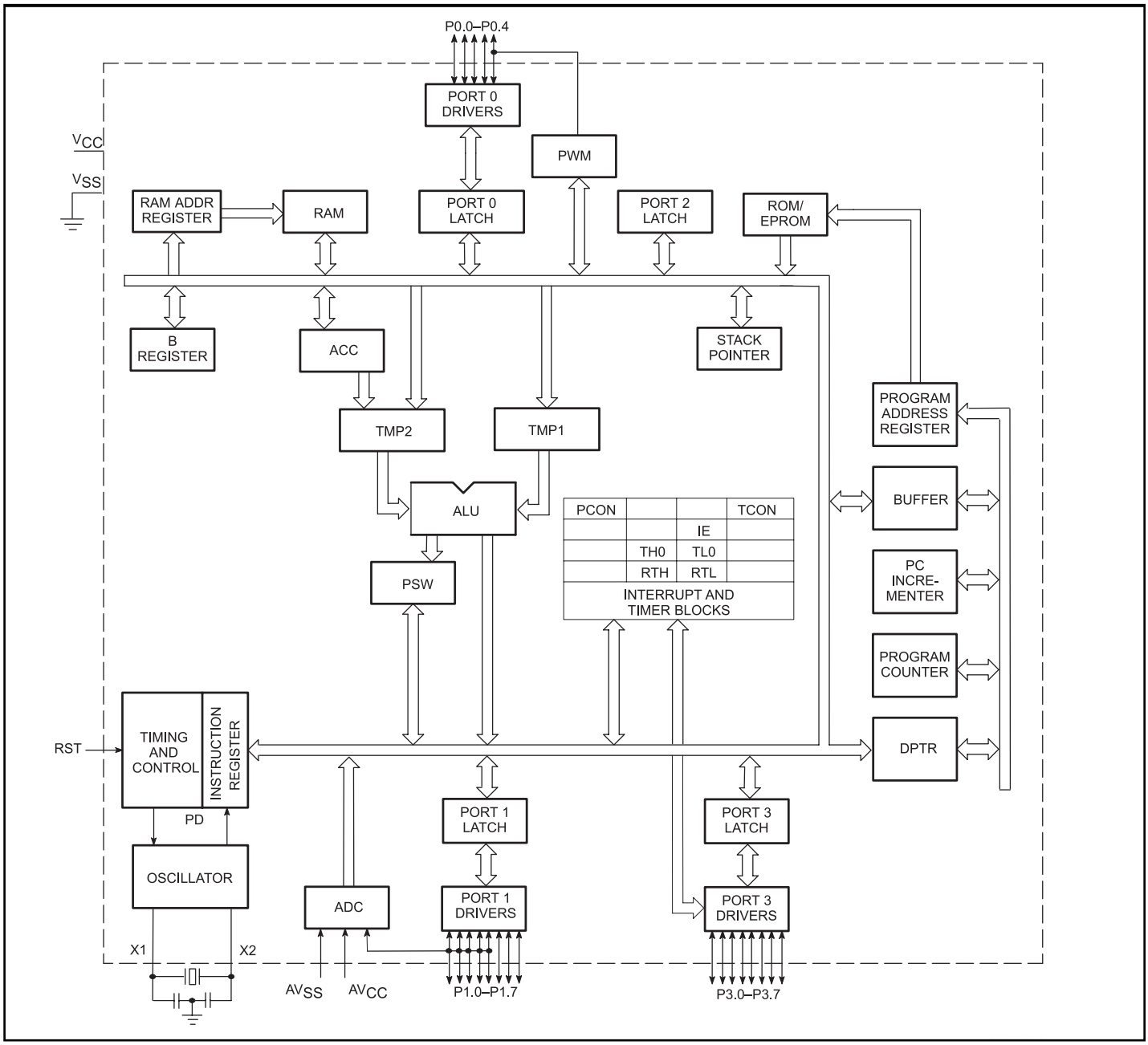

Figure 1: TK87C749 Block Diagram

5. Pin Configuration

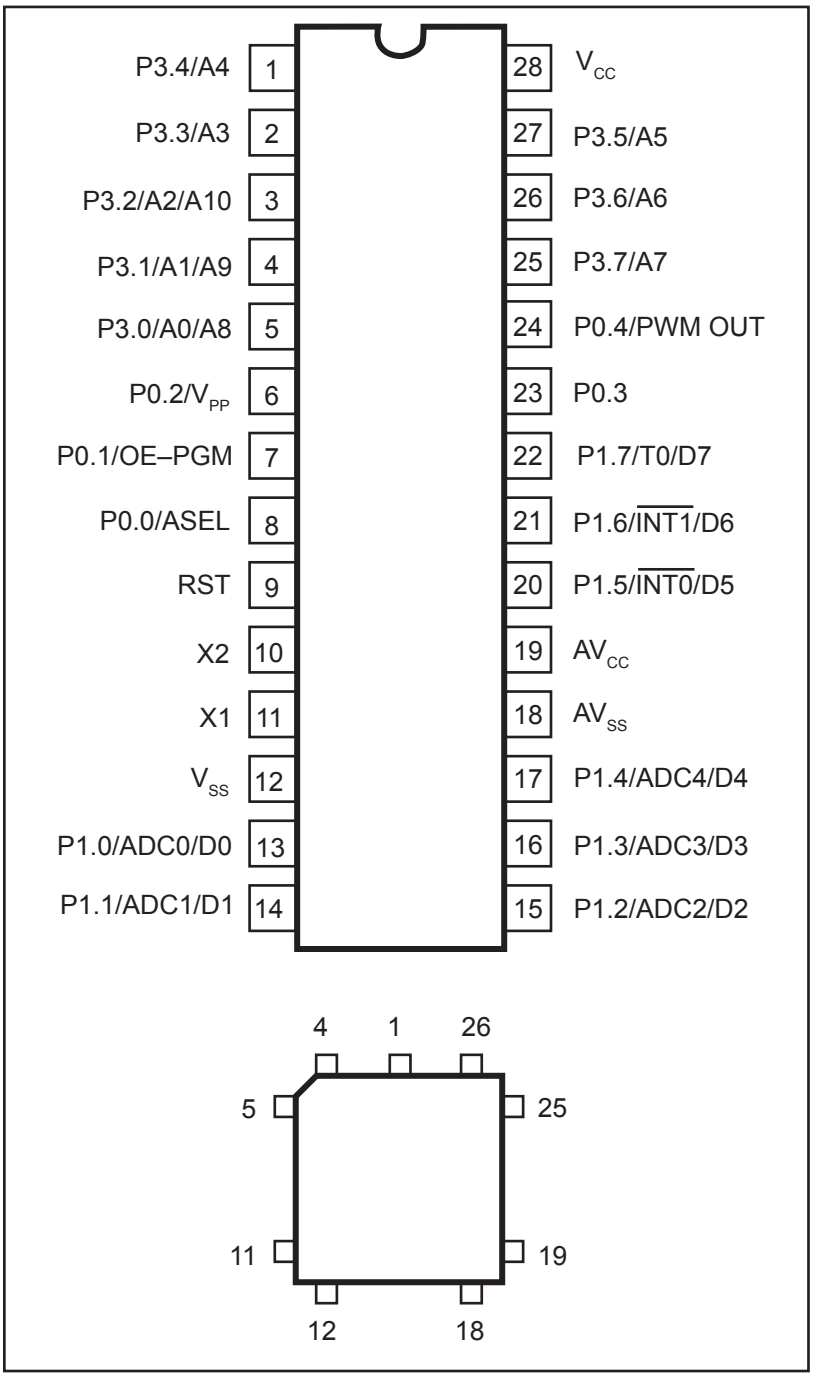

Figure 2: TK87C749 Configuration

Pin	Function	Pin	Function
1	P3.4/A4	15	P1.2/ADC2/D2
2	P3.3/A3	16	P1.3/ADC3/D3
3	P3.2/A2/A10	17	P1.4/ADC4/D4
4	P3.1/A1/A9	18	AV_{SS}
5	P3.0/A0/A8	19	AV_{CC}
6	$P0.2/V_{PP}$	20	P1.5/$\overline{INT0}$/D5
7	P0.1/OE-PGM	21	P1.6/$\overline{INT1}$/D6
8	P0.0/ASEL	22	P1.7/T0/D7
9	RST	23	P0.3
10	X2	24	P0.4/PWM OUT
11	X1	25	P3.7/A7
12	V_{SS}	26	P3.6/A6
13	P1.0/ADC0/D0	27	P3.5/A5
14	P1.1/ADC1/D1	28	V_{CC}

Table 2: TK87C749 Pin Functionality

6. Pin Description

Mnemonic	Pin No.	Type	Name and Function
V_{SS}	12	I	**Circuit Ground Potential.**
V_{CC}	28	I	**Supply voltage during normal, idle, and power-down operation.**
P0.0–P0.4	8–6 23, 24	I/O	**Port 0:** P0 is a 5-bit bidirectional port, while P0.0−P0.2 are open drain ports. All 1s written to P0.0−P0.2 automatically float and can function as high-impedance inputs in this condition. P0.3–P0.4 are also bidirectional I/O port pins. As internal pull-up resistors, these pins are driven low if the port register bit is inscribed with a 0. The program's port register can always read the pin's state. Identically to P3, P0.3–0.4 can be used as inputs and draw pins inscribed with 1s. Despite minor differences, P0.0 and P0.1 are similar enough to "standard TTL" features for the pins to function as general-purpose I/O.
	6	I	**V_{PP} (P0.2) –** Programming voltage input. Internal ROM operation may be impacted when P.0 is near 0 V. For best results, tie P0.2 to V_{CC} with a small pullup (e.g., 2KΩ).
	7	I	**OE/PGM (P0.1) –** Input that specifies either verify (output enable) or program mode. OE / PGM = 1 output enabled (verify mode). OE / PGM = 0 program mode.
P1.0–P1.7	13–17, 20–22	I/O	**Port 1:** P1 is an 8-bit bidirectional I/O port. Its internal pull-ups can function as inputs, pulling high pins inscribed with 1s. P0.3–P0.4 pins are bidirectional I/O port pins with internal pull-ups. As inputs, internal pull-ups cause the current to flow out of externally low P1 pins (see DC Electrical Characteristics). The TK80C51 family also highlights P1 as a special function feature:
	20	I	**$\overline{\text{INT0}}$ (P1.5):** External interrupt.
	21	I	**$\overline{\text{INT1}}$ (P1.6):** External interrupt.
	22	I	**T0 (P1.7):** Timer 0 external input.
	13–17	I	**ACC0 (P1.0)–ADC4 (P1.4):** P1 is the input to the five channel multiplexed A/D converter. These pins serve as digital inputs when the A/D function is enabled and outputs when the A/D function is disabled.
P3.0–P3.7	5–1, 27–25	I/O	**Port 3:** P3 is an 8-bit bidirectional I/O port with internal pull-ups. These internal pull-ups attract P3 pins inscribed with 1s so the pins function as inputs. As inputs, internal pull-ups cause the current to flow out of externally low P3 pins (see DC Electrical Characteristics: I_{IL}). P0.0 / ASEL refers to the 11-bit address multiplexed into this port.
RST	9	I	**Reset:** To reset this device, set this pin on high for two machine cycles during oscillator operation. To power-on RESET an internal diffused resistor to V_{SS}, use an external capacitator to V_{CC}. After reset, a 10-bit serial sequence sent LSB first sets the device in programming mode. This mode uses the programming address, data, and V_{PP} for programming and verification. Synchronize the RESET serial sequence with the X1 input.
X1	11	I	**Crystal 1:** Input to the inverting oscillator amplifier and internal clock generator circuits. X1 is the clock strobing a serial bit stream into RESET, setting the device in programming mode.
X2	10	O	**Crystal 2:** Output from the inverting oscillator amplifier.
AV_{CC}[1]	19	I	**Analog supply voltage and reference input.**
AV_{SS}[2]	18	I	**Analog supply and reference ground.**

Table 3: TK87C749 Pin Description

AV_{SS} (reference ground) must be connected to 0 V (ground). AV_{CC} (reference input) cannot differ from V_{CC} by more than ± 0.2 V and must be in the range 4.5 V to 5.5 V.

7. Oscillator Characteristics

X1 and X2 are input and output pins to an inverting amplifier, which can function as an on-chip oscillator. To drive the device from an external clock source, apply the X1 pin but leave X2 disconnected. No requirements exist for the external clock signal's duty cycle because the internal clock circuitry input channels through a divide-by-two flip-flop. However, programmers must still observe minimum and maximum high and low times specified in this data sheet.

8. Idle Mode

Much like the TK80C51, the TK8XC749 comes with a power-down mode and idle mode. Idle mode causes the CPU, A/D, and PWM to go to sleep while Timer 0, Timer 1, and the interrupts continue to run. When going to sleep, normal operating mode gives the instruction to enable idle mode last. The CPU contents, the on-chip RAM, and the special function registers (SFRs) all remain intact during this process.

There are two ways to reactivate the chip: an enabled interrupt or a hardware reset. During an enabled interrupt, the interrupt service routine will recover and resume the process. A hardware reset triggers the processor similarly to a power-on reset. When leaving idle mode, stabilize the internal analog reference voltages before beginning an A/D conversion.

8.1 Special Function Registers

The SFRs are nearly identical to the directly addressable TK8XC751 registers, except for the program counter and four register blanks, which are not included. The 21 SFRs mainly control the chip's exterior hardware. Other registers include arithmetic registers (ACC, B, PSW), stack pointer (SP) and data pointer registers (DPH, DPL). Nine of the SFRs are bit addressable.

8.2 Data Pointer

Two bytes make up the data pointer (DPTR): a high byte (DPH) and a low byte (DPL). In the TK80C51, the MOVX instruction enables the register to access external data memory. The TK83C749 does not support MOVX or external memory accesses but uses an MOVC instruction, where the register functions as the accumulator's 16-bit offset pointer. The DPTR also works as two independent 8-bit registers.

9. Power Down Mode

Power-down mode stops the oscillator. Normal operating mode executes this command last during shutdown. Whereas idle mode maintained the CPU contents, on-chip RAM, and SFRs, power-down mode only preserves the on-chip RAM contents. Resetting the hardware is the only way to restart the chip. The PCON SFR contains the control bits for reduced power modes.

Mode	Port 0	Port 1	Port 2
Idle	Data	Data	Data
Power-down	Data	Data	Data

Table 4: External Pin Status During Idle & Power-Down

Table 4 does not refer to the PWM output (P0.4).

10. TK87C749 Vs. TK80C51

10.1 Program Memory

The TK8XC749's memory is only 2,048 bytes long and cannot expand. As a result, it will not correctly execute the TK80C51 MOVX, LJMP, and LCALL instructions. No operation will occur, even though the correct number of instruction cycles and external fetches occur. The LJMP may not answer to all program address bits. There are only two fixed locations in program memory:

1. Addresses responding to reset, and
2. Interrupts.

See Table 5 for a list of events triggering interrupts:

Event	Program Memory Address
Reset	000
External $\overline{\text{INT0}}$	003
Counter/timer 0	00B
External $\overline{\text{INT1}}$	013
Timer I	01B
ADC	02B
PWM	033

Table 5: Events Triggering Interrupts

10.2 Memory Output

The TK8XC749 manipulates operands in three memory spaces: program memory space, internal data memory, and SFRs.

Program memory has 2k bytes of address space and includes program instructions and constants (e.g., look-up tables). Internal data memory has a 128-byte logical address space, but the TK8XC749 only applies the first 64 bytes (0 to 3FH).

The third space, an SFR array, also has a 128-byte address space (80H to FFH) but only uses selected locations (see Table 11). Aside from the amount of applied memory, these memory spaces have an identical architecture to the TK80C51.

Because the TK8XC749 does not directly address external data or program memory spaces, it does not implement the TK80C51 MOVX instructions or alternate I/O pin functions RD and WR.

10.3 I/O Ports

The TK83C749 has three I/O pins: P0, P1, and P3.

Port 0. P0, a 5-bit bidirectional I/O port, includes several pins with alternate functions. For example, P0.3 and P0.4 have internal pull-ups, and P0.0, P0.1, and P0.2 are equipped with open drain output structures. P0.4 can also serve as a PWM output.If the alternate function of PWM is not being used, then this pin may function as an I/O port.

Port 1. P1, an 8-bit bidirectional I/O port, has identical architecture to the TK80C51. All pins belonging to P1 have alternate input functions, as shown below:

P1.0-P1.4—ADC0-ADC4	A/D converter analog inputs
P1.5 $\overline{\text{INT0}}$	External interrupt 0 input
P1.6 $\overline{\text{INT1}}$	External interrupt 1 input
P1.7—T0	Timer 0 external input

$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, or T0 can operate as standard I/O ports when their alternate functions are not in use. To utilize P1.5, P1.6, and P1.7 as standard I/O pins, connect AV_{CC} and AV_{SS} to V_{CC} and V_{SS}.

While the A/D converter is enabled, the analog channel connected to the A/D will not work as a digital input. Remaining analog inputs can function as digital inputs but not as digital outputs. Analog inputs will float under these conditions.

Port 3. P3, an 8-bit bidirectional I/O port, has the same structure as the TK80C51. Alternate functions associated with TK80C51's P3 now exist in P1 of the TK83C749, as applicable. See Figure 3 for port bit configurations.

10.4 Counter / Timer Subsystem

Timer / counter 0 is the only counter / timer in the TK8XC749. It is similar to mode 2 in the TK80C51 but is extended 16 bits with 16 bits of auto load. The counter also includes centralized controls found in the TCON register.

Timer I Implementation. At 10 bits wide, Timer I is clocked once per machine cycle (the oscillator frequency divided by 12). To enable the timer, set the TIRUN bit (bit 4) in the I2CFG register. Stop and clear the timer by inscribing a 0 into the TIRUN bit.

When the timer reaches a 1024 terminal count, it carries out and executes the interrupt flag. Bit ETI (bit 4) of the Interrupt Enable (IE) register causes interrupts to occur. Bit EA (bit 7) from the same IE register performs global interrupts. To clear the interrupt flag, set the CKRTI bit (bit 5) in the I1CFG register.

The interrupt service routine must start at 1Bhex, the Timer I vector address. Interrupt will only push the Program Counter onto the stack, which is true for the entire TK8051 family. Only registers used both by the interrupt service routine and elsewhere must be explicitly saved.

10.5 Interrupt Subsystem—Fixed Priority

The interrupt subsystem eliminates both the IP register and the 2-level interrupt system of the TK80C51. The interrupt structure is a seven-source, one-level interrupt system similar to the TK8XC751.

As shown below, this system resolves simultaneous interrupt conditions using a single-level, fixed priority:

Highest priority:	Pin $\overline{\text{INT0}}$
	Counter/timer flag 0
	Pin $\overline{\text{INT1}}$
	PWM
	Timer I
Lowest priority:	ADC

The vector addresses are as follows:

Source	Vector Address
INT0	0003H
TF0	000BH
INT1	0013H
TIMER I	001BH
ADC	002BH
PWM	0033H

Table 6: Vector Addresses

Position	Symbol	Function
IE.7	EA	Global interrupt disable when EA=0
IE.6	EAD	A/D conversion complete
IE.5	ETI	Timer I
IE.4	—	N/A
IE.3	EPWM	PWM counter overflow
IE.2	EX1	External interrupt 1
IE.1	ET0	Timer 0 overflow
IE.0	EX0	External interrupt 0

Table 7: Interrupt Enable Registers

Interrupt Control Registers. The TK80C51 interrupt enable register accounts for the TK8XC749's different interrupt sources.

Interrupt Enable Register.

MSB							LSB
EA	EAD	ETI	—	EPWM	EX1	ET0	EX0

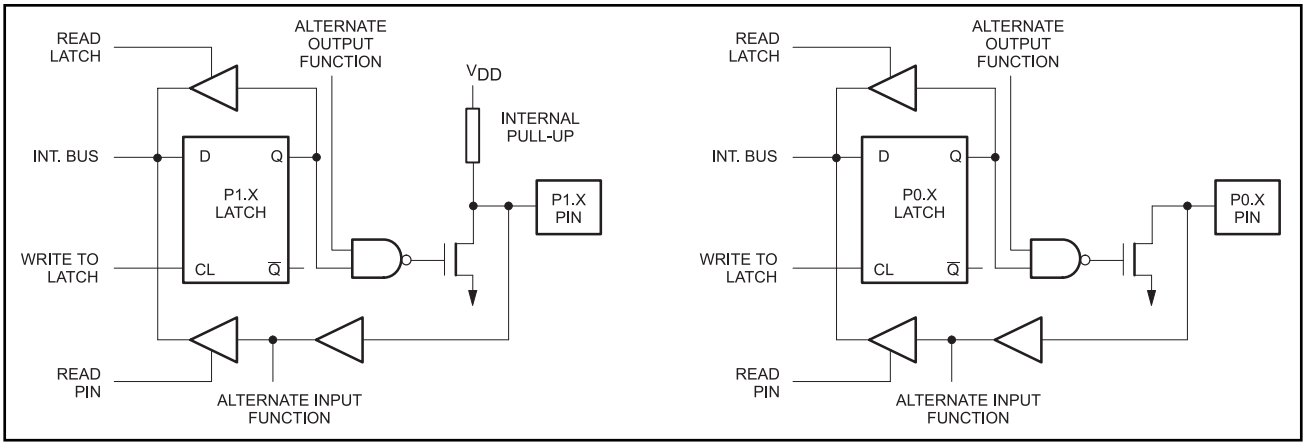

Figure 3: Port Bit Latches & I/O Buffers

10.6 Pulse Width Modulation Output (P0.4)

The Pulse Width Modulation (PWM) function transmits pulses with length and interval programmable options. An 8-bit prescaler sets the repetition frequency and generates the clock for the counter.

The prescaler register (PWMP) and counter are only associated with counter / timer 0. The 8-bit counter counts modulo 255, ranging from 0 to 254 inclusive. The counter equates its value with the PWM, which serves as a compare register. The PWM output is set high when the counter value equals this register's contents; however, the output is set low when the counter reaches zero. The compare register's contents determine the pulse width ratio (duty cycle). This cycle ranges from 0 to 1 and is programmed in increments of 1/255. To set the PWM output as continuously high, load the compare register with 0. To set the output as continuously low, load the compare register with 255.

A bit in an SFR (PWENA) enables the PWM output. When enabled, the pin output is driven with a fully active pull-up (i.e., the PWM uses a strong

pull-up when its output is high). When disabled, the pin works like a standard bidirectional I/O pin, but the counter is still active.

To disable PWM, execute the RESET command. After the reset clears, PWM will remain disabled until software enables it to restart. The PWM output is high during power-down and idle modes. Idle mode disables the counter. The PWM's repetition frequency is given by:

$$f_{PWM} = f_{OSC} / 2 (1 + PWMP) 255$$

When PWM ≠ 255, the PWM signal's high / low ratio is PWM / 255 – PWM). When PWM = 255, the output is always low.

An oscillator frequency of 12MHz yields a repetition frequency range of 92 Hz – 23.5 kHz.

An interrupt will disturb the PWM counter overflow if not masked off.

P0.4 can also function as a PWM output. To use this port as a bidirectional I/O port, disable PWM by clearing PWENA's enable / disable bit. To use PWM as an interval timer, enable the PWM interrupt.

10.7 Special Function Register Addresses

The SFRs in the TK8XC749 and the TK80C51 are the same, except for a few minor differences.

The TK8XC749 removes the following SFRs:

- TMOD (89),
- P2 (A0), and
- IP (B8).

The TK8XC749 adds the following SFRs:

- ADCON (A0),
- ADAT (84),
- PWM (8E),
- PWMP (8F), and
- PWENA (FE).

10.8 A/D Converter

The analog input circuitry includes a 5-input analog multiplexer and a 5-channel multiplexed 8-bit A/D converter with 8-bit resolution. The conversion prompts the machine to cycle 40 times (40 µs at 12 MHz oscillator frequency).

The ADCON control register regulates the A/D converter. The analog multiplexer uses ADCON register bits 0–2 to select input channels. The ADCON register is not bit addressable.

ADCON Register.

MSB							LSB
X	X	ENADC	ADCI	ADCS	AADR2	AADR1	AADR0

ADCI	ADCS	Operation
0	0	ADC free; can start a conversation.
0	1	ADC busy; cannot begin new conversations.
1	0	Conversion complete; cannot begin new conversations.
1	1	Not possible.

Table 8: ADCI / ADCS Operation

Address 2	Address 1	Address 0	Input Pin
0	0	0	P1.0
0	0	1	P1.1
0	1	0	P1.2
0	1	1	P1.3
1	0	0	P1.4

Table 9: Input Channel Selection

The ADCON register's ADCI indicates when the 8-bit ADC conversion is finished, logging the outcome in the ADAT SFR. An ADC START will not impact an ADC conversion already in progress.

This is also true for completed conversions, provided the ADCI = logic 1. When ADCS or ADCI = logic 1, new ADC STARTS are blocked and deleted as a result.

Starting idle or power-down mode will terminate ADC conversions in progress. However, idle mode will not affect completed conversion results (ADCI = logic 1). Figure 4 displays the corresponding circuit for an A/D input.

Position	Symbol	Function
ADCON.5	ENADC	Enable A/D function when ENADC = 1. If reset, ENADC = 0.
ADCON.4	ADCI	ADC interrupt flag. Sets when ADC conversion completes. Requests an interrupt when IE.6 and ADCI = 1.The ADCI flag clears when conversion data is read. ADCI is read only.
ADCON.3	ADCS	ADC starts A/D conversion. Once set, ADCS remains high during cycle. When finished, it resets before ADCI interrupt flag clears. Software cannot reset ADCS. Use ADCI, not ADCS, to monitor the A/D converter status.
ADCON.2	AADR2	Analog input select.
ADCON.1	AADR1	Analog input select.
ADCON.0	AADR0	Analog input select. The binary coded address selects one of P1's five analog input port pins to be input to the converter. Only changes when ADCI and ADCS are both low. AADR2 is the most significant bit.

Table 10: ADCON Control Registers

When a 0 disables the A/D converter in the ADCON's ENADC bit, analog input pins ADC0–ADC4 can operate as digital inputs or outputs. However, the analog input channel selected by ADDR2–ADDR0 in ADCON will not function as a digital input if A/D is enabled. A/D always returns a 1 as a digital input.

Unselected A/D inputs also work as digital inputs, but unselected analog inputs float and therefore cannot function as digital outputs.

The TK8XC749 A/D reference inputs connect to the AV_{CC} and AV_{SS} analog supply pins. As a result, the A/D reference voltage will always be identical to the analog supply pins' voltage. Ensure AV_{SS} links to 0 V, and AV_{CC} links to a supply voltage ranging from 4.5–5.5 V. A/D measurements must also range from 4.5–5.5 V. Do not increase the A/D ground reference voltage above 0 V or reduce the positive A/D reference voltage below 4.5 V.

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function								Reset Value
			MSB							LSB	
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
ADAT#	A/D result	84H									00H
ADCON#	A/D control	A0H	–	–	ENADC	ADCI	ADCS	AADR2	AADR1	AADR0	C0H
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data pointer (2 bytes)	82H 83H									00H
DPL	Data pointer low										00H
DPH	Data pointer high		AF	AE	AD	AC	AB	AA	A9	A8	
IE*#	Interrupt enable	ADH	EA	EAD	ETI	—	EPWM	EX1	ET0	EX0	00H
			–	–	–	84	83	83	81	80	
P0*#	Port 0	80H	–	–	–	PWM0	–	–	–	–	xxx11111B
			97	96	95	94	93	92	91	90	FFH
P1*#	Port 1	90H	T0	INT1	INT0	ADC4	ADC3	ADC2	ADC1	ADC0	
P3*	Port 3	B0H	B7	B6	B5	B4	B3	B2	B1	B0	FFH
PCON#	Power control	87H	–	–	–	–	–	–	PD	IDL	xxxx0000B
			D7	D6	D5	D4	D3	D2	D1	D0	

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
PWCM#	PWM compare	8EH									xxxxxxxxB
PWENA#	PWM enable	FEH	–	–	–	–	–	–	–	PWE	FEH
PWMP#	PWM prescaler	8FH									00H
RTL#	Timer low reload	8BH									00H
RTH#	Timer high reload	8DH									00H
SP	Stack pointer	81H									07H
TL#	Timer low	8AH									00H
TH#	Timer high	8CH									00H
			DF	DE	DD	DC	DB	DA	D9	D8	
TICON*#	Timer I control	D8H/RD	–	–	0	TIRUN	–	–	–	–	0000xx00B
		WR	–	–	CLTRI	TIRUN	–	–	–	–	
			8F	8E	8D	8C	8B	8A	89	88	
TCON*#	Timer control	88H	GATE	C/T	TF	TR	IE0	IT0	IE1	IT1	00H

Table 11: TK87C749 Special Function Registers

* SFRs are bit addressable.
# SFRs are modified from or added to the TK80C51 SFRs.

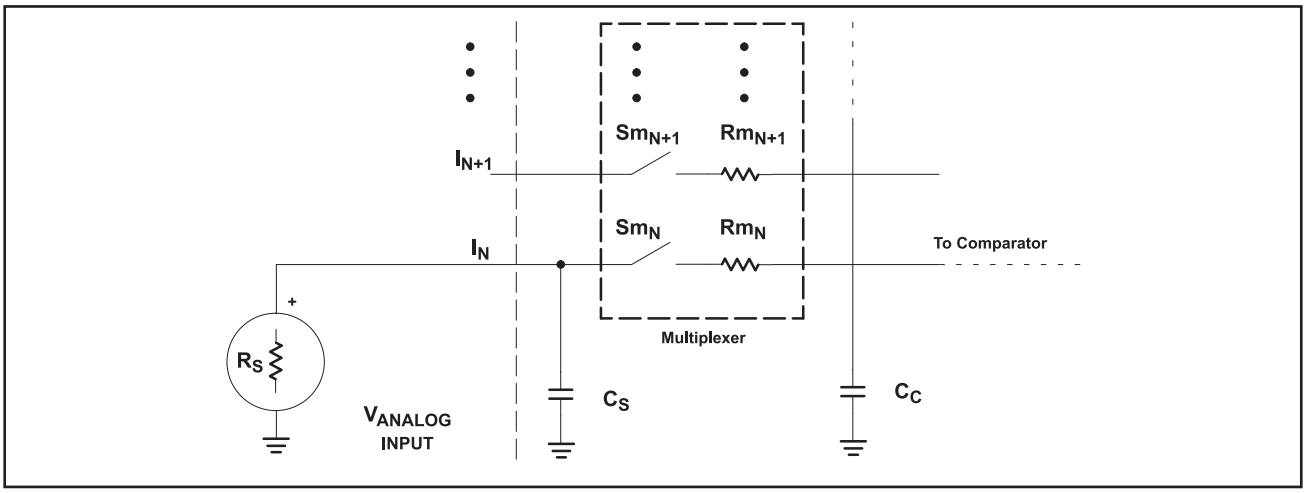

Figure 4: A/D Input: Equivalent Circuit

Rm = 0.5 - 3 kΩ
CS + CC = 15 pF maximum
RS = Recommended < 9.6 kΩ for LSB @ 12 MHz

Because the analog to digital converter has a sampled-data comparator, the input looks capacitive to a source. When a conversion is initiated, switch Sm closes for 8tcy (8 µs @ 12 MHz crystal frequency) during which time capacitance Cs + Cc is charged. The sampling causes the analog input to present a varying load to an analog source.

11. A/D Converter Parameter Definitions

The following definitions clarify some select specifications but do not represent all A/D parameter definitions.

11.1 Absolute Accuracy Error

Absolute accuracy error of a given output is the difference between the expected analog output and the actual output when applying a given digital code. A band of input voltages produce identical output codes; therefore, the “required input voltage” equals the midpoint of the input voltage band producing that code. The maximum over all codes refers to any absolute accuracy error that the code does not specify.

11.2 Non-Linearity

Non-linearity is the maximum deviation between the ideal output of a digital-to-analog converter (DAC) and the actual output level. For example, if one draws a line between two converter characteristic endpoints and subtracts zero offset and full-scale errors, then non-linearity equals the maximum deviation of the characteristic’s code transitions. Other terms for non-linearity include *relative accuracy* and *integral non-linearity.*

11.3 Differential Non-Linearity

Differential non-linearity (DNL) is the deviation between two analog values corresponding to adjacent input digital values. DNL equals the maximum difference between the actual and ideal converter code widths. Code widths are LSB-defined variances between the code transition points. These differences occur when the input voltage fluctuates within the code set range.

11.4 Gain Error

Gain error is the variance between the ideal and actual analog input voltage. Once the offset error is removed, this value helps convert the final code to a full-scale output code.

11.5 Offset Error

Offset error, also known as full-scale error, is the difference between the actual and ideal input voltage needed to trigger the first code transition. This ideal value = 1/2 LSB above V_{ref-}.

11.6 Channel-to-Channel Matching

Channel-to-channel matching measures the maxmum difference between code transitions of actual characteristics and code transitions of other channels. Measurements use the same temperature, voltage, and frequency conditions of actual characteristics so that values are comparable.

11.7 Crosstalk

Crosstalk is the unwanted transfer of signals between communication channels. More specifically, a deselected channel receives a signal, causing the converter to output. Crosstalk measures the level of that signal.

11.8 Total Error

Total error is the maximum deviation of any step point from a line connecting the ideal first and last transition points.

11.9 Relative Accuracy

Relative accuracy error is the deviation between the ADC’s actual and ideal code transition points on a straight line. Offset error and gain error are null. This type of error uses LSBs or FSR percentage expression.

12. Counter/Timer

Timer 0, the TK8XC749 counter / timer, is different from Timer I and the PWM. It works similarly to the TK80C51 mode 2 and extends to 16 bits. As an external counter, Timer 0 samples the T0 input (P1.7) every S4P1. The timer control register (TCON) regulates the counter/timer.

MSB							LSB
GATE	C/T	TF	TR	IE0	IT0	IE1	IT

Position	Symbol	Function
TCON.7	GATE	1 – Timer 0 is enabled only when INT0 is high and TR = 1. 0 – Timer 0 activates when TR = 1.
TCON.6	C/T	1 – Counter operation from T0 pin. 0 – Internal clock timer operation.
TCON.5	TF	1 – Set on overflow of T0. 0 – Cleared when processor vectors to interrupt routine and by reset.
TCON.4	TR	1 – Enable timer 0. 0 – Disable timer 0.
TCON.3	IE0	1 – Edge detected on INT0.
TCON.2	IT0	1 – INT0 is edge triggered. 0 – INT0 is level sensitive.
TCON.1	IE1	1 – Edge detected on INT1.
TCON.0	IT1	1 – INT1 is edge triggered. 0 – INT1 is level sensitive.

Table 12: TKON Flag Operation

The TKON flags and the TK80C51 operate nearly the same, except the flags share the same register and have only one TK80C51 style timer.

The IE0 / IT0 and IE1 / IT1 bit positions are opposite of the standard TK80C51 TCON register positions.

Timer I can function as a fixed base timer or watchdog timer. On the other hand, Timer 0 is a 16-bit auto-reloadable timer / counter comparable to TK80C51 mode 2. Either the oscillator frequency or T0 pin transitions will meter the timer / counter at a 1/12 rate.

The C/T bit in SFR TCON picks between oscillator frequency mode and T0 pin transition mode. Setting the TCON TR bit activates the timer / counter. The clock source increments register pair TH and TL. When the register pair overflows, it takes values from RTH and RTL registers, leaving the reload register values untouched.

The TF bit in SFR TCON is set on counter overflow and causes an interrupt if the interrupt is activated (see Figure 5).

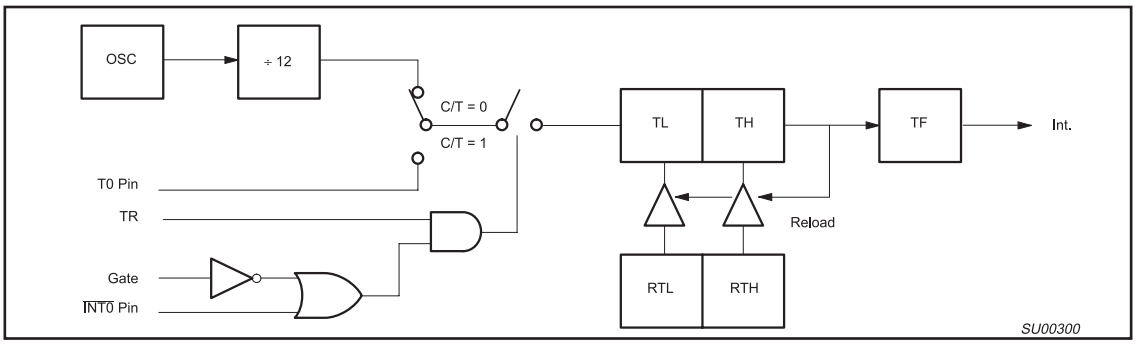

Figure 5: TK83C749 Counter/Timer Block Diagram

Parameter	Rating	Unit
Storage temperature range	–65 to +150	°C
Voltage from V_{CC} to V_{SS}	–0.5 to +6.5	V
Voltage from any pin to V_{SS} (except V_{PP})	–0.5 to V_{CC} + 0.5	V
Power dissipation	1.0	W
Voltage from V_{PP} pin to V_{SS}	–0.5 to + 13.0	V

Table 13: Absolute Maximum Ratings

13. DC Electrical Characteristics

T_{amb} = 0°C to +70°C, AV_{CC} = 5V ±5, AV_{SS} = 0V[4]
V_{CC} = 5V ± 10%, V_{SS} = 0V

Symbol	Parameter	Test Conditions	Limits[4]			Unit
			MIN	TYP[1]	MAX	
I_{CC}	Supply current (See Figure 8)					
Inputs						
V_{IL}	Input low voltage	(0 to 70°C)	–0.5		$0.2V_{CC}$–0.1	V
V_{IH}	Input high voltage, except X1, RST	(0 to 70°C)	0.2_{CC}+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage, X1, RST	(0 to 70°C)	$0.7V_{CC}$		V_{CC}+0.5	V
	P0.2					
V_{IL1}	Input low voltage	(0 to 70°C)	–0.5		$0.3V_{CC}$	V
V_{IH2}	Input high voltage	(0 to 70°C)	$0.7V_{CC}$		V_{CC}+0.5	V
Outputs						
V_{OL}	Output low voltage, ports 1, 3, 0.3, and 0.4 (PWM disabled)	I_{OL} = 1.6mA[2]			0.45	V
V_{OL1}	Output low voltage, port 0.2	I_{OL} = 3.2mA[2]			0.45	V
V_{OH}	Output high voltage, ports 1, 3, 0.3, and 0.4 (PWM disabled)	I_{OH} = –60µA, I_{OH} = –25µA I_{OH} = –10µA	2.4 $0.75V_{CC}$ $0.9V_{CC}$			V V V
V_{OH2}	Output high voltage, P0.4 (PWM enabled)	I_{OH} = –400µA I_{OH} = –40µA	2.4 $0.9V_{CC}$			V V
V_{OL2}	Port 0.0 and 0.1 - Drivers Output low voltage	I_{OL} = 3mA (over V_{CC} range)			0.4	V
C	Driver, receiver combined: Capacitance				10	pF
I_{IL}	Logical 0 input current, ports 1, 3, 0.3, and 0.4 (PM disabled)[11]	V_{IN} = 0.45V (0 to 70°C)			–50	µA
I_{TL}	Logical 1 to 0 transition current, ports 1, 3, 0.3 and 0.4[11]	V_{IN} = 2V (0 to 70°C)			–650	µA
I_{LI}	Input leakage current, port 0.0, 0.1, and 0.2	0.45 < V_{IN} < V_{CC}			±10	µA
R_{RST}	Reset pull-down resistor		25		175	kΩ
C_{IO}	Pin capacitance	Test freq = 1MHz, T_{amb} = 25°C			10	pF

I_{PD}	Power-down current[5]	V_{CC} = 2 to 5.5V V_{CC} = 2 to 6.0V (TK83C749)			50	µA
V_{PP}	VPP program voltage (TK87C749 only)	V_{SS}=0V V_{CC}=5V ±10% T_{amb}=21°C to 27°C	12.5		13.0	V
I_{PP}	Program current (TK87C749)	V_{PP} = 13.0V			50	mA

Symbol	Parameter	Test Conditions	Limits[4]			Unit
			Min.	Type[1]	Max.	
Analog Inputs (A/D guaranteed only with quartz window covered.)						
AV_{CC}	Analog supply voltage[10]	$AV_{CC}=V_{CC}$ ±0.2V	4.5		5.5	V
AI_{CC}	Analog operating supply current	AV_{CC} = 5.12V			3[9]	mA
AV_{IN}	Analog input voltage		AV_{SS}–0.2		AV_{CC}+0.2	V
C_{IA}	Analog input capacitance				15	pF
t_{ADS}	Sampling time				$8t_{CY}$	s
t_{ADC}	Conversion time				$40t_{CY}$	s
R	Resolution				8	bits
E_{RA}	Relative accuracy				±1	LSB
OS_e	Zero Scale Offset				±1	LSB
G_e	Full scale gain error				0.4	%
M_{CTC}	Channel to channel matching				±1	LSB
C_t	Crosstalk	0–100kHz			–60	dB

Table 14: DC Electrical Characteristics

1. *Using stresses above the Absolute Maximum Ratings recommendation can permanently damage the device. This is a stress rating only. Only operate the device under conditions outlined in this specification's AC and DC Electrical Characteristics section.*
2. *Externally limit I_{OL} under the following steady state (non-transient) conditions:*

   Maximum I_{OL} per port pin: 10mA (85° C spec.)

   Maximum I_{OL} per 8-bit port: 26mA

   Maximum total I_{OL} for all outputs: 67mA

   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins may not sink current greater than the listed test conditions.

3. *This product's circuitry is designed to protect its internal devices from extreme static charge. Nevertheless, use safeguards to prevent application above recommended limits.*
4. *Parameters can exceed operating temperature range, and all voltages are consistent with V_{SS} unless otherwise noted.*
5. *Output pins are disconnected during power-down I_{CC} measurement; port 0 = V_{CC}; X2, X1 n.c.; RST = V_{SS}.*
6. *I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} – 0.5V; X2 n.c.; RST = port 0 = V_{CC}. I_{CC} will be slightly higher when using a crystal oscillator.*
7. *Idle I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} – 0.5V; X2 n.c.; port 0 = V_{CC}; RST = V_{SS}.*
8. *Load capacitance for ports = 80pF.*
9. *The resistor ladder network is not disconnected in the power down or idle modes. Thus, remove AV_{CC} to conserve power.*
10. *If A/D is not required or used sporadically, detaching the AV_{CC} will not impact digital circuitry operation. ADCON and ADAT contents may not be valid. After detaching AV_{CC}, reduce A/D inputs under 0.5V. P1.0–P1.4 digital inputs will not operate normally.*
11. *When A/D active, these parameters do not apply to P1.0–P1.4.*

14. AC Electrical Characteristics

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ± 10%, V_{SS} = 0V[4, 8]

Symbol	Parameter	16MHz Clock		Variable Clock		Unit
		MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	Oscillator frequency:			3.5	16	MHz
External Clock (Figure 6)						
t_{CHCX}	High time	20		20		ns
t_{CLCX}	Low time	20		20		ns
t_{CLCH}	Rise time		20		20	ns
t_{CHCL}	Fall time		20		20	ns

Table 15: AC Electrical Characteristics

14.1 Explanation of the AC Symbols

Each timing symbol contains five characters, the first of which is always ‘t’ (= time). The other characters specify a signal’s name or logical status, depending on their positions. Here are their designations:

C – Clock
D – Input data
H – Logic level high
L – Logic level low
Q – Output data
T – Time
V – Valid
X – No longer a valid logic level
Z – Float

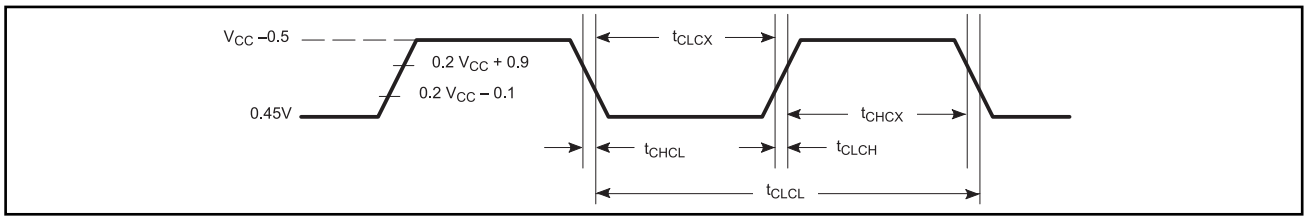

Figure 6: External Clock Diagram

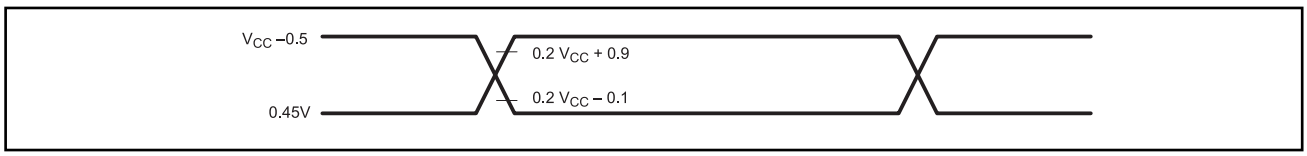

Figure 7: AC Testing Input/Output

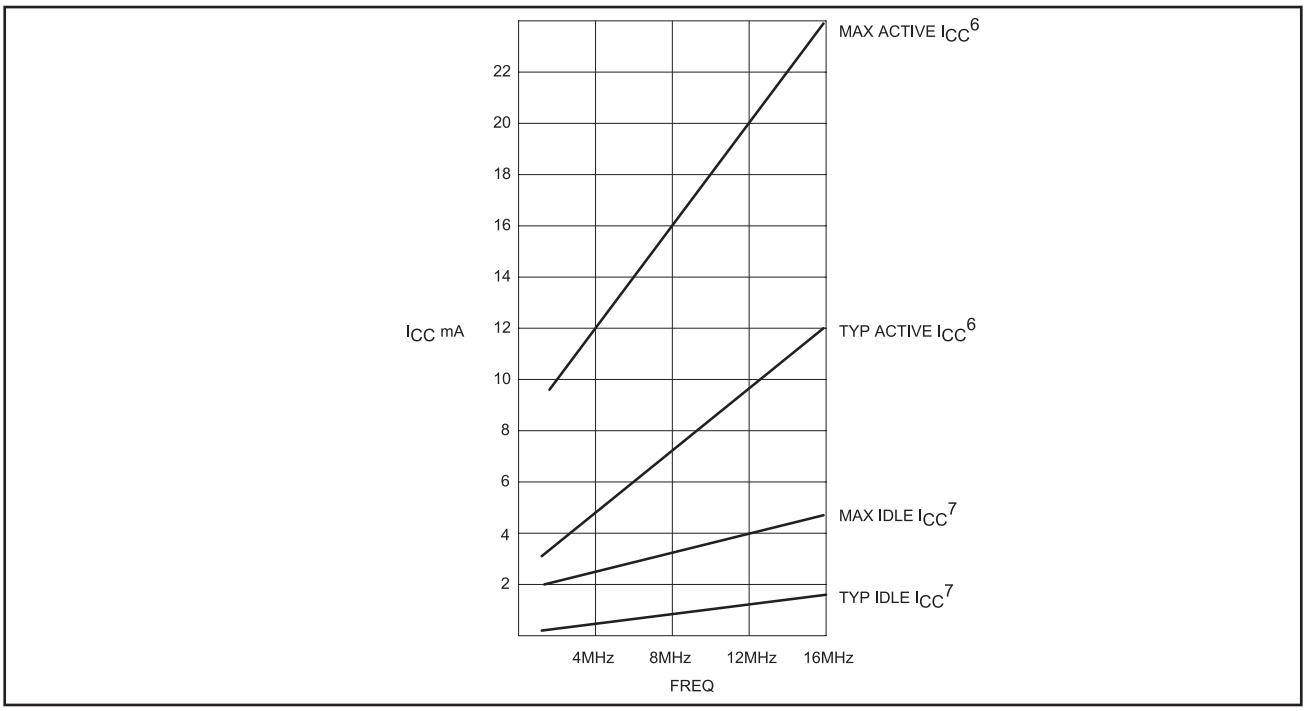

Figure 8: I_{cc} vs. FREQ

Maximum I_{CC} values taken at V_{CC} = 5.5 V and worst case temperature. Typical I_{CC} values taken at V_{CC} = 5.0 V and 25° C.

15. Flash Considerations

15.1 Overview

Tekmos replaced the OTP EPROM in the original 87C751 with a 64 KB Flash memory. This alteration allows much more programming flexibility for new designs while still maintaining backwards compatibility for existing designs. However, since Flash is not EPROM, the programming procedures are different.

This part must be programmed in a dedicated programmer. ISP and IAP are not supported at this time. Flash can be programmed either through Tekmos' or the third party providing programming support.

The Flash memory uses the chip's 5-volt supply for all programming voltages. High programming voltages are not required and should never be applied to the chip.

15.2 Driving the Clock

The TK83C749 has a 2-pin crystal oscillator on pins X1 (P13) and X2 (P12). X1 is the input, and X2 is the output. The internal clock is derived from the X2 pin, and so at a minimum, the X2 pin should be left open. The capacitive load on X2 causes a timing delay between the X1 pin and the internal clock. When a capacitive load burdens X2, it may be necessary to drive the X2 pin using the X1 signal.

15.3 Flash Mode

The TK83C749 is put into the programming mode in the same manner as the original chip. Program the clocks to run continuously. On the falling edge of the reset, a 10-bit word (296 h) LSB first, is shifted into the reset pin, using X1 as the clock.

Data is clocked internally on the rising edge of X1. Changing the input data on the falling edge of X1 provides ample setup and holdup times.

After receiving the Flash Mode command, the part enters Flash Mode, and the part pins are redefined as follows:

Pin	Function
Port 1	Data Bus
Port 3	Address Bus
P0.0	Address Strobe
P0.1	WEn (0 = Write)
P0.2	OE (1 = Read)
X1	Clock

Table 16: Flash Mode Pin Assignments

15.4 Addressing

The internal flash has 512 KB of storage and requires a full 19-bit address. However, the application only uses the lower 16 address bits. The upper address bits must be set to zero.

The TK83C749 provies an 8-bit address bus. In order to provide the full 19-bit address from the Flash, the TK83C749 has two internal address latches used to hold the upper address bits. The address strobe shifts address data into these latches.

When P0.0 (address strobe) goes high, then the data on P3 is clocked with the falling edge of XTAL1 into the lower address latch (A8–A15), and the contents of the lower address latch are clocked into the upper address latch (A16–A23).

To set up an address, first clock in A16–A23, then clock in A8–A15. The P3 pins become A0–A7.

15.5 Reading the Flash

With OE high, the contents of the Flash appear on P1. Note that the lower address can be changed without affecting the upper address lines. This allows the read of 256 addresses without having to write the upper address lines.

The internal flash has an access time of 90 ns. Another 20 ns is required for the address setup and the data output. As a result, the maximum output data rate is approximately 8 MHz.

15.6 Flash Busy

When A23 = 1, bit D0 becomes the Flash busy signal. This transformation allows the chip to monitor the Flash status during the chip erase command.

15.7 Flash Write Operations

Writing to the Flash consists of loading the desired address, bringing the P0.2 pin (OE) low, putting the desired data on Port 1, and pulsing the P0.1 pin (WEn) low.

A single write is ineffective. The Flash memory contains multiple interlocks to prevent accidental data writes. These interlocks take the form of Flash commands. A command is a sequence of 4–6 consecutive write operations.

15.8 Erasing the Flash

Erase Flash using the following commands:

Cycle	Address	Data
1	000AAh	AAh
2	000555h	55h
3	000AAAh	80h
4	000AAAh	AAh
5	000555h	55h
6	000AAAh	10h

Table 17: Flash Erase

It typically takes 1–10 seconds for the Flash to erase. For best results, monitor the busy pin to determine when the erase cycle is complete.

15.9 Writing to the Flash

Bytes may be written to the Flash with a 4-cycle write as follows:

Cycle	Address	Data
1	000AAAh	AAh
2	000555h	55h
3	000AAAh	A0h
4	Address	Data

Table 18: Flash Byte Write

15.10 Burst Mode

When programming large amounts of data, the Flash memory may transition into Burst Mode. This mode consists of an unlock command, multiple data writes, and a lock command, which terminates the procedure. Upper address registers do not need to be programmed with each byte write, which reduces a byte write from 12 clocks to 2 clocks.

On every 256-byte boundary, rewrite upper address bits to the correct value.To instigate Burst Mode, send the the unlock command, as shown below:

Cycle	Address	Data
1	000AAAh	AAh
2	000555h	55h
3	000AAAh	20h

Table 19: Flash Unlock

Next, write each byte in a 2-cycle sequence. This may be repeated as many times as needed.

Cycle	Address	Data
1	000AAAh	AAh
2	000555h	55h

Table 20: Flash Burst Data Write

Finish by sending the lock command:

Cycle	Address	Data
1	XXXXXXh	90h
2	XXXXXXh	F0h

Table 21: Flash Lock

15.11 Encryption Array and Security Bits

At this time, the TK83C749 does not support the e ncryption array or the two security bits.

16. Programming Operation

Figures 10–11 show the timing diagrams for the program / verify cycle. Hold RESET high for at least two machine cycles. The RESET operation causes P0.1 (PGM/) and P0.2 (V_{PP}) to rest at V_{OH}. At this time, the pins act as normal, quasi-bidirectional I/O ports, which may cause the programming equipment to pull these lines low. However, the equipment should drive P0.1 and P0.2 high (V_{IH}) before sending the RESET pin's 10-bit code.

The RESET pin can now serve as the data stream's serial data input, which activates programming mode. Because data bits are sampled when the clock is high, they should only change when the clock is low. Hold the RESET pin low after transmitting the last data bit.

Next, place the address information for the programming location on P3. Use ASEL to multiplex the address, as described previously. P1 will now work as an output. To program P1 as an input port, apply a high voltage V_{PP} level to the V_{PP} input (P0.2). Then apply a series of programming pulses to the PGM/ pin (P0.1). These pulses are created by driving P0.1 low and then high. This pulse is repeated until a total of 25 programming pulses have occurred. At the conclusion of the last pulse, the PGM/ signal should remain high. Generate these pulses by driving P0.1 low and then high.

Repeat the pulse 25 times. The PGM/ signal should stay high after the last pulse. To use P1 as an output, drive the V_{PP} signal to the V_{OH} level, which activates verify mode.

To begin the next programming cycle, place the address information at the multiplexed buffer inputs, which drives the V_{PP} pin to the V_{PP} voltage level. This brings the programmable byte to P1, releases 26 pulses on the PGM/ pin, and returns the V_{PP} to the V_C level, verifying the byte.

16.1 Programming / Verifying Security Bits

Program security bits using port pin serial data streams and logic levels. P1 and P3 do not need address or data information during programming.

The verification process uses the RESET serial stream (see Table 22). It is not necessary to drive P3. P1.6 and P1.7 will display the verify operation results. P1.7 includes the security bit 1 data, and P1.6 includes the security bit 2 data. P1.7 and P1.6 both equal logic 1 if programmed and logic 0 if not programmed.

Operation	Serial Code	P0.1 (PGM/)	P0.2(V_{PP})
Program security bit 1	29AH	–*	V_{PP}
Program security bit 2	298H	–*	V_{PP}
Verify security bits	29AH	V_{IH}	V_{IH}

Table 22: Implementing Program / Verify Modes

*Pulsed from V_{IH} to V_{IL} and returned to V_{IH}.

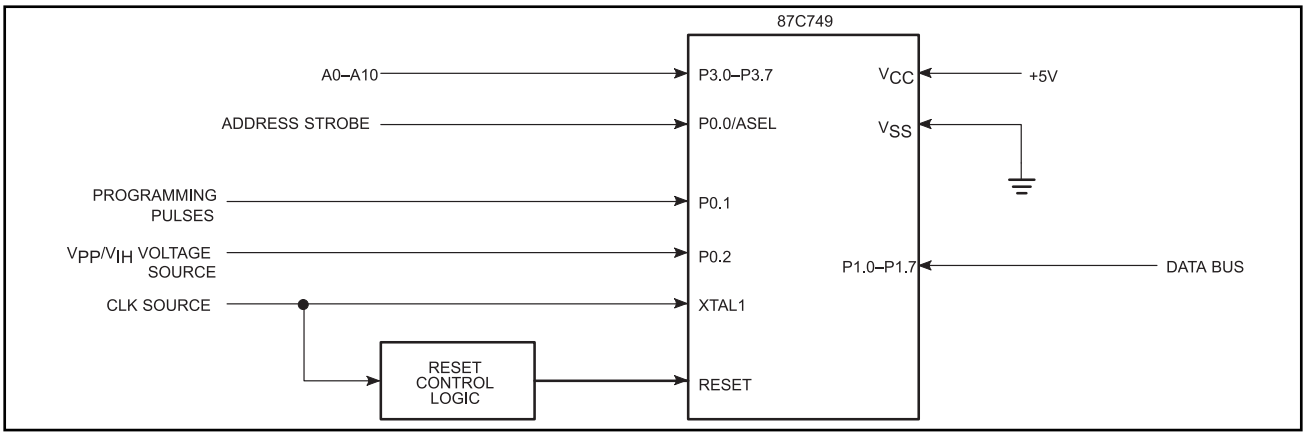

Figure 9: Programming Configuration

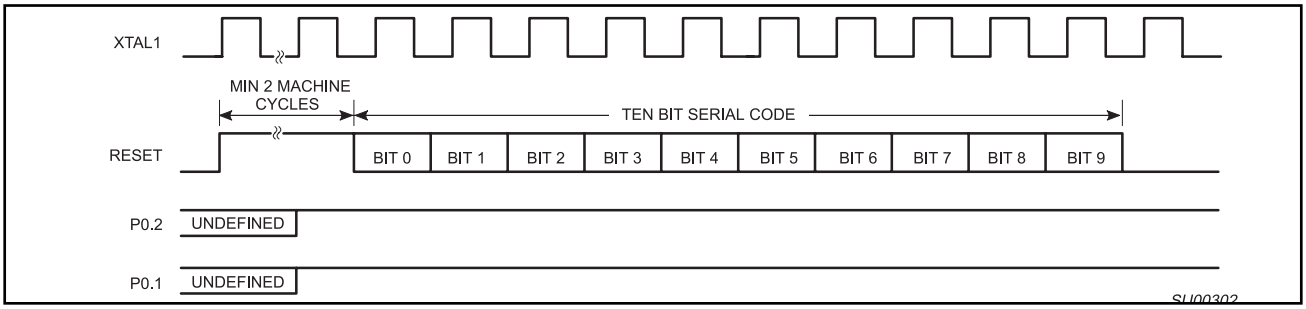

Figure 10: Entry into Program/Verify Modes

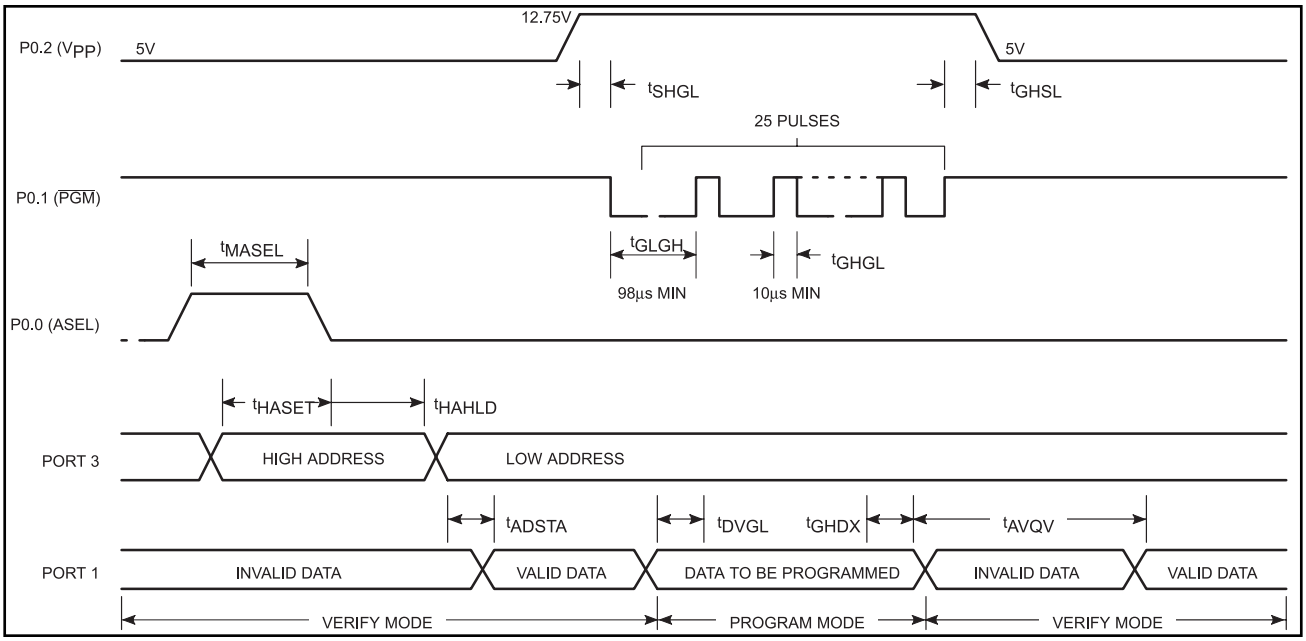

Figure 11: Program/Verify Cycle

17. DIP28: plastic dual in-line package; 28 leads (600 mil); long

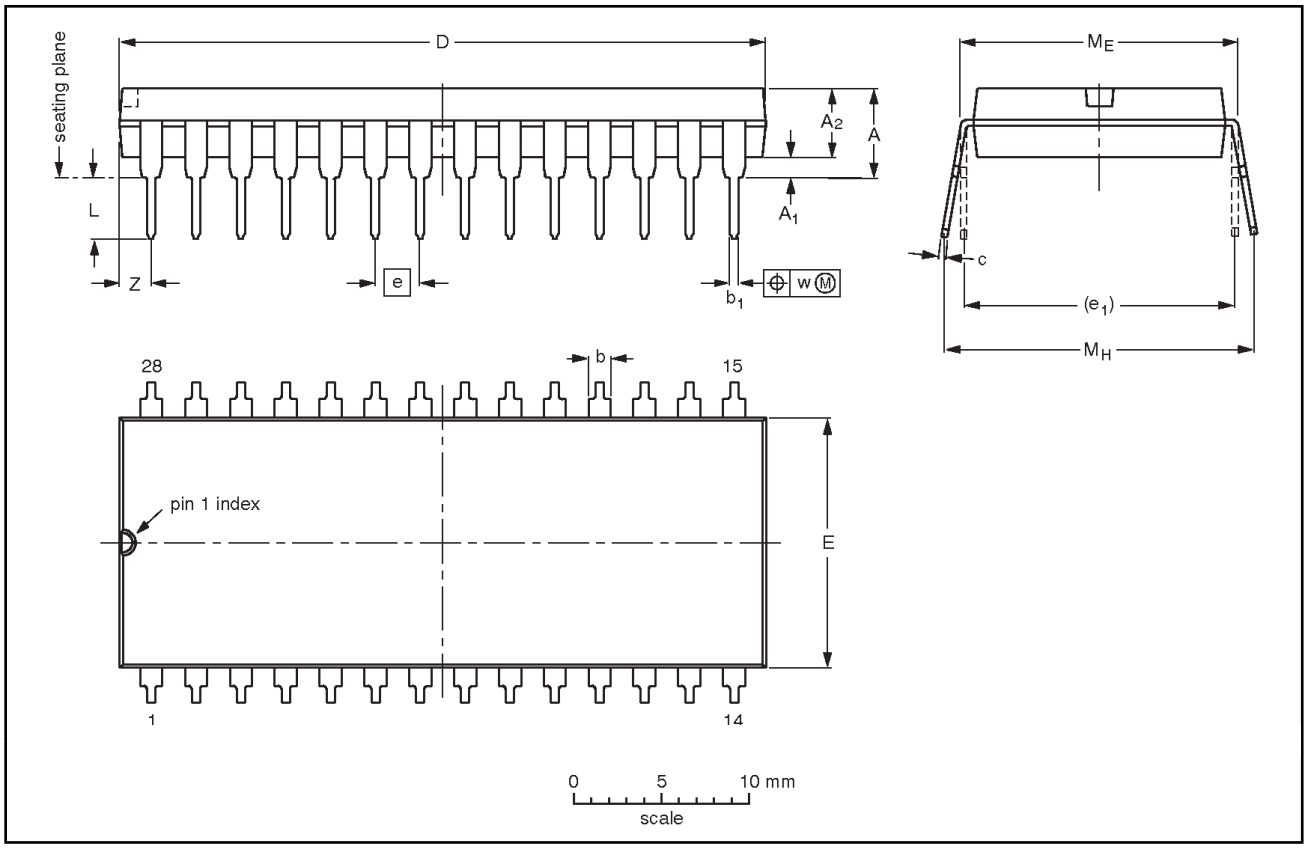

Figure 12: DIP28 Specifications

UNIT	A max.	A_1 min.	A_2 max	b	b_1	c	D(1)	E(1)	e	e_1	L	M_E	M_H	w	Z(1) max.
mm.	5.08	0.51	3.94	1.63 1.14	0.56 0.43	0.38 0.25	37.08 35.94	14.22 13.84	2.54	15.24	3.51 3.05	15.75 15.24	17.65 15.24	0.25	2.10
in.	0.200	0.020	0.155	0.064 0.045	0.022 0.017	0.015 0.010	1.460 1.415	0.560 0.545	0.100	0.600	0.138 0.120	0.62 0.60	0.695 0.600	0.01	0.083

Table 23: DIP28 Dimensions

Millimetre dimensions are derived from the original inch dimensions.

18. PLCC28: plastic leaded chip carrier; 28 leads; pedestal

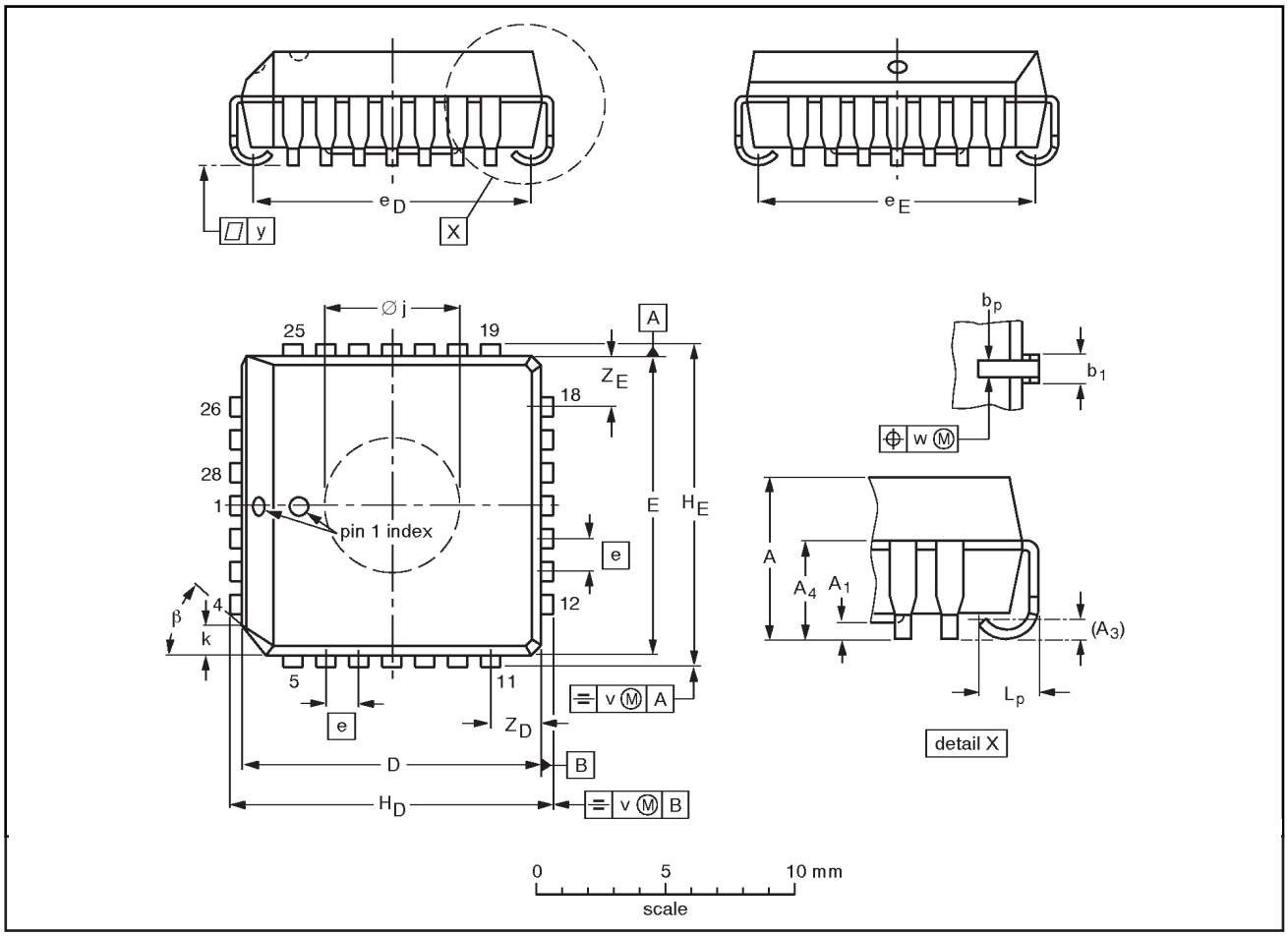

Figure 13: PLCC28 Specifications

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D_{(1)}$	$E_{(1)}$	e	e_D	e_E	H_D	H_E	k	$Ø_j$	L_p
mm.	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	5.69 5.54	1.44 1.02
in.	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.224 0.218	0.057 0.040

UNIT (cont.)	v	w	y	$Z_{D(1)}$ max	$Z_{E(1)}$ max	β
mm	0.18	0.018	0.10	2.06	2.06	45°
in.	0.007	0.007	0.004	0.081	0.081	

Table 24: PLCC28 Dimensions

1. *Millimetre dimensions are derived from the original inch dimensions.*
2. *Plastic or metal protrusions of 0.01 inches maximum per side are not included.*

19. SSOP28: plastic shrink small outline package; 28 leads; body width: 5.3mm

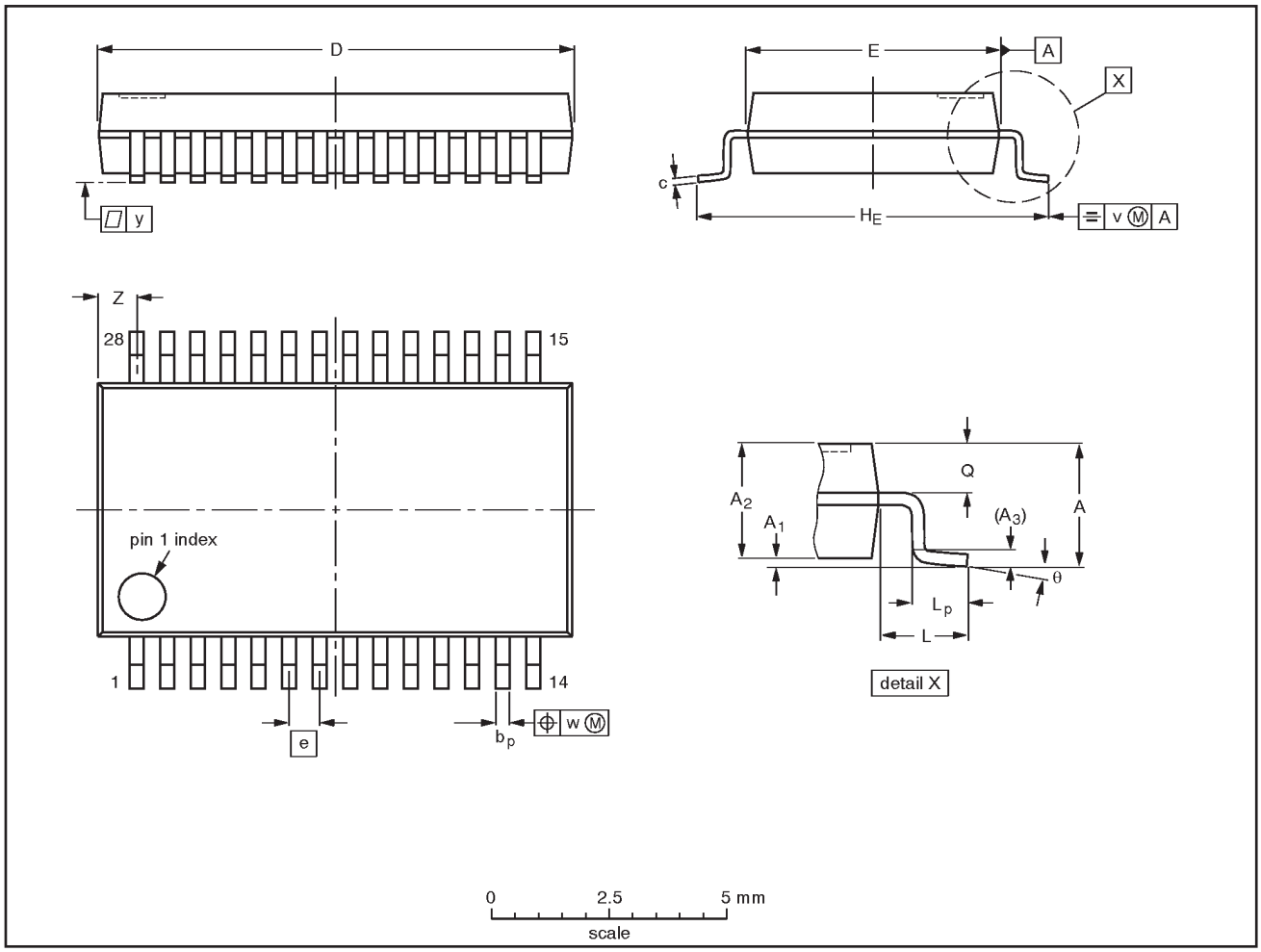

Figure 14: SSOP28 Specifications

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm.	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

Table 25: SSOP28 Dimensions

Plastic or metal protrusions of 0.20 mm maximum per side are not included.