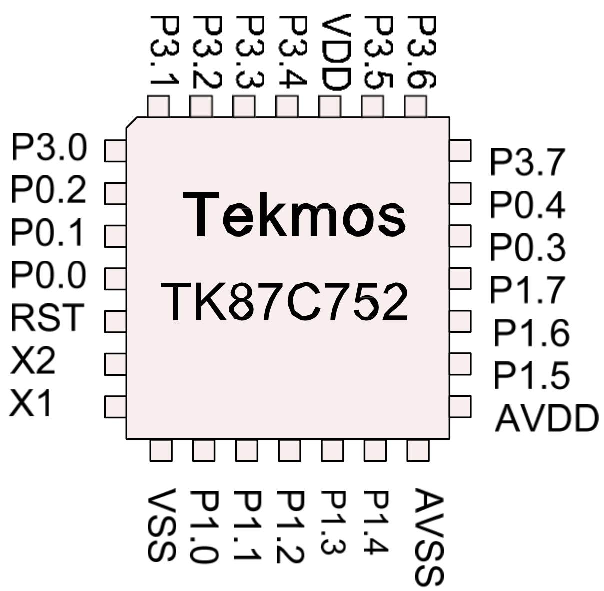
TK87C752
80C51 Microprocessor, 64K Flash

(v2.1) May 14th, 2024 Data Sheet

Features

- 8 Bit Microcomputer with 8051 architecture
- 64Kx8 internal Flash, 256x8 RAM
- Low standby current at full supply voltage
- 0-20 MHz operation
- Classic architecture instruction timing
- 3 bidirectional ports (19 bits)
- 24 pin, 300 mil DIP or 28 pin PLCC package
- Built in power management
- Two Wire Interface (TWI) (I2C™ compatible)
- 16 bit timer/counter with auto-reload.
- 8-bit PWM
- Fixed rate timer
- 8-bit ADC with 5 channels
- LED compatible outputs
- Direct replacement for Philips 83C752 / 87C752 microprocessors.
- Implemented with the Tekmos Customer Configured Microprocessor (CCM) technology.



General Description

The TK87C752 is a derivative of the 8051 microprocessor architecture. With 64Kx8 of mask programmed ROM, and 256x8 of scratchpad RAM, this part is a pin-for-pin replacement of the Philips 87C752 microprocessor.

The TK87C752 is intended to provide the 80C51 architecture in a small package and with a hardware Two Wire Interface (TWI). The integrated TWI interface allows the TK87C752 to operate as either a master or a slave on the TWI bus.

To achieve this, port P2, and 5 bits of port P0 were removed, along with the external bus control pins. This allows the TK87C752 to fit within either a 28 pin, 300 mil PDIP package, or a 28 pin PLCC package.

The 8051 architecture has been modified to provide a Two-Wire Interface (TWI). Starting with the basic 80C51 design, the serial port and the two timers in the 80C51 were removed and replaced with the TWI interface and its associated timers. The external interrupt pins and the timer gate and count pins were relocated from port P3 to port P1. The interrupt controller was simplified to provide only a single set of priorities.

The ability of the design to access external program and data memory was also removed, along with the PSEN, ALE, and EA pins.

The TK87C752 is built utilizing the Tekmos Customer Configured Microprocessor (CCM) technology. Refer to the CCM data sheet for details on creating other microprocessors.

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Pin Descriptions

PLCC	PDIP	Name	Description
1	1	P3.4	Port 3. Bit 4
2	2	P3.3	Port 3. Bit 3
3	3	P3.2	Port 3. Bit 2
4	4	P3.1	Port 3. Bit 1
5	5	P3.0	Port 3. Bit 0
6	6	P0.2	Port 0. Bit 2
7	7	P0.1 / SDA	Port 0. Bit 1 + TWI data
8	8	P0.0 / SCL	Port 0. Bit 0 + TWI clock
9	9	RST	Active high reset
10	10	XTAL2	Crystal Oscillator Output
11	11	XTAL1	Clock / Crystal Oscillator Input
12	12	VSS	Ground
13	13	P1.0	Port 1. Bit 0 + ADC Channel 0
14	14	P1.1	Port 1. Bit 1 + ADC Channel 1
15	15	P1.2	Port 1. Bit 2 + ADC Channel 2
16	16	P1.3	Port 1. Bit 3 + ADC Channel 3
17	17	P1.4	Port 1. Bit 4 + ADC Channel 4
18	18	AVDD	Analog Vdd
19	19	AVSS	Analog Vss
20	18	P1.5 / INT0n	Port 1. Bit 5 + External interrupt 0
21	19	P1.6 / INT1n	Port 1. Bit 6 + External interrupt 1
22	20	P1.7 / T0	Port 1. Bit 7 + Timer 0 clock / gate
23	23	P0.3	Port 0. Bit 3
24	24	P0.4 / PWM	Port 0. Bit 4 + PWM Out
25	25	P3.7	Port 3. Bit 7
26	26	P3.6	Port 3. Bit 6
27	27	P3.5	Port 3. Bit 5
28	28	VDD	Positive Supply

Architecture

The TK87C752 architecture consists of a classic 8051 core controller surrounded by the TWI controller, three general purpose I/O ports, two timer counters, an interrupt controller, 64 bytes of RAM, and 2K bytes of ROM.

8051 Core

The 8051 core, register set, instructions, and timing are the same as in the classic 8051.

The MOVX instructions exist, but are meaningless since the TK87C752 cannot access external memory. Likewise, the data pointers (DPTR) are still present, but serve no purpose other than general purpose registers.

I/O Ports

The TK87C752 has 3 of the original 4 8-bit bidirectional I/O ports. Ports 1 and 3 are the same as in the classic 8051. Port 0 has been reduced to 5 bits, and port 2 has been removed. All ports are mapped into the SFR address space and may be directly operated on by instructions. The port bits are configured as bidirectional pins. Writing a 1 to the port allows that bit to be configured as an input.

Port 0

Port 0 has been reduced to 5 bits. Bits 0 to 2 are bidirectional – open drain pins. The TWI interfaces through P0.0 (SCK) and P0.1 (SDA). These pins are stronger so as to meet the electrical requirements of the TWI bus. Bits 3 and 4 are bidirectional with an internal pull-up.

P0 - Port 0		
Pin	Name	Alternate Function
P0.0	SCK	TWI Clock
P0.1	SDA	TWI Data
P0.2		
P0.3		
P0.4	PWM	PWM Output

Port 0 is located at address 80H.

Port 1

These bits are bidirectional pins, with a pullup present on all pins. Many of the special function controls that were on Port 3 in the original 8051 have been relocated to Port 1. The following table shows the new bit assignments.

P1 - Port 1		
Pin	Name	Alternate Function
P1.0	ADC0	ADC Channel 0
P1.1	ADC1	ADC Channel 1
P1.2	ADC2	ADC Channel 2
P1.3	ADC3	ADC Channel 3
P1.4	ADC4	ADC Channel 4
P1.5	INT0	External Interrupt 0
P1.6	INT1	External Interrupt 1
P1.7	T0	Timer 0 Clock / Gate

Port 1 is located at address 90H.

Port 2

Port 2 has been removed from the design.

Port 3

Port 3 pins serve as a parallel I/O port. The SFR functions present in the 801 have been moved to Port 1.

Port 3 is located at address B0H.

Read-Modify-Write Instructions

Since each port pin is configured as an open-drain, it is possible for the contents of the port latch to differ from the value at the pin. Instructions that read the port reference the value at the pin. An exception to this is a set of instructions that perform a read-modify-write function. These instructions read the contents of the port latch, modify it, and write it back out. The read-modify-write instructions are:

ANL	JBC
CLR B	MOV B, C
CPL	ORL
DEC	SET B
DJNZ	XRL
INC	

Precharge

Bits 0-2 in Port 0 are configured as bidirectional open-drain when it is used as a port.

Ports 1, 3, P0.3 and P0.4 have an internal pull-up resistor on each pin. In addition, whenever a port makes a 0 to a 1 transition, a precharge occurs for two crystal clock cycles. This precharge improves the rise times of the port pins. The precharge also occurs during the alternate port functions.

Serial Port

The serial port and the associated special function registers have been removed from the TK87C752.

Timers

The Timer 0 and Timer 1 functions in the classic 8051 have been extensively modified for use in the TK87C752. The TK87C752 has two timers: Timer 0 is a 16-bit timer/counter. Timer I is a 10-bit fixed- rate timer.

The operation of Timer 0 is similar to the mode 2 operation in the classic 8051, but with 16 bits. Timer 0 is clocked by either T0 externally, or by 1/12 of the oscillator frequency internally. This is controlled by the C/T pin in special function register TCON. Timer 0 is enabled when the TCON TR (Timer Run) bit is set.

The clock source increments the TL and TH register pair. When the register pair overflows, it is reloaded with the contents of the RTL and RTH register pair. The reload value does not change. See the TK87C752 counter/timer block diagram for further details. When Timer 0 overflows, it sets the TF bit in the TCON register. This will generate an interrupt if the interrupt has been enabled.

Clock Control

There is considerable flexibility in the control of the clock for either timer. The C/T bit in the TCON register selects the source of the clock. Setting it to a one selects the external T0 pin as a clock source, while clearing it to a zero selects the internal clock.

After the source has been selected, it is further controlled by the TR bit of the TCON register. Clearing this bit blocks the clock and prevents operation. Setting the bit enables the clock.

The clock can also be controlled by the GATEn bit in the TCON register. Setting this bit allows the external interrupt pin to gate the clock. A 1 on the external interrupt pin enables the clock.

The clock controls act as an enable on the clock generator. This prevents spurious clocks from being generated when the controls are switched.

Clock Speed

When operating off the internal clock source, the timers will be incremented once every machine cycle. Since there are twelve external clocks per machine cycle, the maximum count frequency is Fosc/12.

External pins are sampled once per machine cycle. If the external clock source is selected, it will take two machine cycles to create a complete clock waveform, thus making the maximum external clock frequency Fosc/24. While there are no limitations on the external clock duty cycle, care must be taken to insure that the clock signal has been sampled correctly during the S5P2 time. This is easily accomplished by maintaining the external timer clock in a given state for a minimum of one machine cycle.

Interrupts

The setting of the TF bit in the TCON register triggers an interrupt request. The TF bit is reset by hardware when the requested interrupt is acknowledged.

The TCON register also controls the external interrupts. These functions are explained in the interrupt section.

The Timer Data Registers

Each timer consists of a lower register (TL) and an upper register (TH). These registers are treated as any other SFR register and may be read from or written to at any time. These registers are unbuffered and represent the current count value.
The data registers are mapped into the SFR address space at the following locations:

Register	Address
TL	8AH
RTL	8BH
TH	8CH
RTH	8DH

The Timer Control Register

With the removal of Timer 1, the remaining control functions have been consolidated in the TCON register. The TMOD register has been removed. As with the data registers, the control registers may be treated as any other SFR register, and may be read from or written to at any time.

The TCON register controls the enable for Timer 0, the timer interrupt bit, the edge selects for external interrupts and the external interrupt bits. Interrupt bits generate the interrupt and may be set by software as well as hardware. Here are the bit assignments for the TCON register. Note that the bit positions are different than those used in the classic 8051.

Address = 88h
Reset value = 00h

TCON – Timer Control Register		
Pin	Name	Function
TCON.7	GATE	Timer 0 Clock / Gate
TCON.6	C/T	Counter / Timer Mode
TCON.5	TF	Timer Flag
TCON.4	TR	Timer Run
TCON.3	IE0	External Interrupt 0
TCON.2	IT0	INT0 Edge Select
TCON.1	IE1	External Interrupt 1
TCON.0	IT1	INT0 Edge Select

GATE

1 = Timer enabled when INT0 and TR are high.
0 = Timer enabled by TR only.

C/T Counter / Timer

1 = Clock from external T0 pin.
0 = Clock from internal clock.

TF – Timer Flag

1 = Overflow occurred on TH, request interrupt.

This bit is cleared by the interrupt acknowledge.

TR – Timer Run

1 = Timer runs
0 = Timer off

IE0

1 = Interrupt detected on INT0
0 = No interrupt on INT0

IT0

1 = Interrupt on falling edge of INT0
0 = Interrupt on INT0 = 0

IE1

1 = Interrupt detected on INT1
0 = No interrupt on INT1

IT1

1 = Interrupt on falling edge of INT1
0 = Interrupt on INT0 = 1

Two Wire Interface

The Two Wire Interface (TWI) uses bidirectional clock (SCK) and data (SDA) lines to transfer data between multiple devices. In the TK87C752, the TWI logic contains hardware to simplify the software required to interface with the bus. The hardware is a single bit interface that includes bus arbitration logic, framing error detect, clock stretching, and a timer for bus timeout. The hardware interfaces to the software through either interrupts or polling.

Timer I

Timer I controls the six critical time spans in the TWI architecture. These are:

1. The minimum high time for SCL when in master mode.
2. The minimum low time for SCL when in master mode.
3. The minimum SCL high to SDA high time for a stop bit.
4. The minimum SDA high to SDA low time between stop and start bits.
5. The minimum SDA low to SCL low time in a start bit.
6. The maximum SCL change time within a frame.

The three low order bits of timer I control the first 5 times. Selecting the appropriate value based on the oscillator speed will allow these times to be the 4.7us required by the TWI specification.

The upper 10 bits of Timer I control the maximum SCL change time. This counter is started by a start bit, cleared by every SCL transition, and turned off by the stop bit. Depending on the preset condition controlled by I2CFG, Timer I will timeout after from 1020 to 1023 machine cycles. At that point, it will clear the TWI hardware, and if enabled, generate an interrupt.

TWI Interrupts

The TWI will try to generate an interrupt when the ATN flag is set. The ATN flag is the OR of four conditions: start, stop, data ready, or loss of arbitration.

Because of the software overhead necessary to determine which condition created the interrupt, it is not practical to use interrupts for the main I2C operation. Instead, it is recommended that interrupts be used to detect a start bit in an idle slave mode, or a stop bit in an idle master mode.

I2CON – TWI Control Register

Address = 98h
Reset value = 81h

I2CON - TWI Control - Write		
Bit	Name	Function
7	CXA	Clear Transmit Active
6	IDLE	Enter idle mode
5	CDR	Clear Data Ready (DRDY)
4	CARL	Clear Arbitration Loss
3	CSTR	Clear Start Bit
2	CSTP	Clear Stop Bit
1	XSTR	Transmit Repeated Start
0	XSTP	Transmit Repeated Stop

I2CON - TWI Control - Read		
Bit	Name	Function
7	RDAT	Receive data
6	ATN	Logical OR of DRDY, ARL, STR, and STP
5	DRDY	Data Ready
4	ARL	Arbitration Loss
3	STR	Start Bit Detected
2	STP	Stop Bit Detected
1	MASTER	Master Mode
0	x	

The bits in the TWI control register (I2CON) have different values, depending on whether the register is being read or written to. As a result, it should **NOT** be used with Read-Modify-Write instructions.

I2CON Register – Write

CXA

Writing a 1 to this bit clears the transmitter active state. This state is also cleared by reading the I2DAT register.

The transmitter active state is entered by writing to the I2DAT register, or by setting the XSTR or XSTP bits in the I2CON register. The TWI must be in the transmitter active state to drive the SDA line low. The transmitter must also be active in order to have the ARL bit set.

The transmitter active state is cleared by either reading the I2DAT register, or by setting the CXA bit. The transmitter active state is automatically cleared with the setting of the ARL bit.

IDLE

Setting the IDLE bit causes a TWI slave to ignore the TWI bus until the next start bit occurs. If MASTRQ is set, then the TWI will become a master after the next stop bit is received.

CDR

Setting this bit clears the DRDY bit. The data ready bit is also cleared by reading or writing the I2DAT register.

CARL

Setting this bit clears the arbitration loss bit (ARL).

CSTR

Setting this bit clears the start bit (STR).

CSTP

Setting this bit clears the stop bit (STP).

Note that if any of the DRDY, ARL, STR or STP bits is set, then the TWI hardware will extend the SCL low time until the bit has been cleared.

XSTR

Setting this bit generates repeated start bits. It should be only used in the master mode. It should not be used to generate the initial start bit in a data packet. That start bit is generated automatically by the TWI hardware.

XSTP

Setting this bit generate a stop bit. It should be only used in the master mode

I2CON Register – Read

RDAT

This bit in the I2CON register is a duplicate of the same bit in the I2DAT register. However, reading the RDAT bit here does not clear the DRDY bit.

In a typical application, the first 7 received bits are read from the I2DAT register. The 8th bit is read here. Then the ACK response is written to the XDAT bit, which clears DRDY.

ATN

The attention bit is high whenever any of the DRDY, ARL, STR, or STP bits is a 1. It provides a single software test for TWI status.

Any of these conditions will extend the SCL low time until they have been cleared. Failure to clear all bits can result in a hung bus.

DRDY

The Data Ready bit is set on the rising edge of SCL, except when the part is operating as an idle slave.

DRDY can be cleared by writing to the CDR bit, or by reading from or writing to the I2DAT register.

Once SDL returns low, it will remain low until the DRDY bit has been cleared.

ARL

ARL = 1 means that an arbitration loss has occurred. The setting of the ARL bit will also clear the transmit active state. There are four conditions that will set the ARL bit.

1. The 87C752 tried to send a 1, but SDA was a zero at the rising edge of SCL.
2. The 87C752 tried to send a 1, but SDA went low while SCL was still high.
3. The 87C752 tried to send a start bit, but another device drove SCL low before the 87C752 could drive SDA low.
4. The 87C752 tried to send a stop bit, but another device was holding the SDA line low.

In any of the above conditions, other bits such as STR or STP may be set, depending on the actual TWI signals.

STR

The STR bit is set when a TWI start condition has been detected on the TWI bus and the TWI hardware is operating as either a non-idle slave or as a master.

STP

The STP bit is set when a TWI stop condition has been detected on the TWI bus and the TWI hardware is operating as either a non-idle slave or as a master.

MASTER

MASTER = 1 indicates that the TWI hardware is currently the master on the WI bus. MASTER is set when MASTRQ is a 1 and the TWI bus is not busy. MASTER is cleared when ARL is set, of after software has cleared the MASTRQ bit, and then set the XSTP bit.

I2DAT – TWI Data Register

Address = 99h
Reset value = 80h

I2DAT - TWI Data		
Bit	Name	Function
7	XDAT RDAT	Transmit Data (Write) Receive Data (Read)
6	x	Not used
5	x	Not used
4	x	Not used
3	x	Not used
2	x	Not used
1	x	Not used
0	x	Not used

XDAT

Transmit data bit. Writing to the XDAT bit defines the next bit to be transmitted on the TWI bus. It also clears the DRDY bit and sets the Transmit Active state.

The XDAT data is only applied to the SDA pin when SCL is low. This prevents the accidental creation of a start or stop bit. It also removes critical timing considerations from the software transmit routines.

RDAT

Receive data bit. This bit is loaded from the SDA pin on every rising edge of SCL. Reading this bit clears the DRDY bit. It also clears the Transmit Active state.

The hardware will delay the rising edge of SCL until the RDAT bit has been read. This removes critical timing considerations from the software receive routines. Of course, the data must be read before Timer I has timed out, which is a minimum of 750 us.

I2CFG – TWI Configuration Register

Address = D8h
Reset value = 0000xx00

I2CFG - TWI Configuration		
Bit	Name	Function
7	SLAVEN	Slave enable
6	MASTRQ	Bus master request
5	CLRTI	Clear Timer I interrupt
4	TIRUN	Timer I run
3	x	Not used
2	x	Not used
1	CT1	Control timer bit 1
0	CT0	Control timer bit 0

SLAVEN

Writing a 1 to the SLAVEN bit puts the TWI interface into the slave mode. This bit is cleared by a TWI time out and reset.

MASTRQ

Setting MASTRQ to a 1 generates a request to become the bus master of the TWI bus. If another bus cycle is in progress, then the TWI waits until a stop bit has been received. Once the bus is available, the TWI sends a start bit and sets the DRDY bit in the I2CON register. This in turn sets the ATN bit and generates an interrupt.

Writing a 1 to the XSTP bit in the I2CON register will release the TWI bus. The MASTRQ bit is cleared by a TWI time out and reset.

The TWI hardware is disabled when both SLAVEN and MASTRQ are 0.

CLRTI

The Timer I interrupt flag is cleared by writing a 1 to this bit. This bit always reads as a 0.

TIRUN

This bit controls Timer I. A 1 allows Timer I to run. A 0 stops and clears Timer I. This bit, along with the SLAVEN, MASTRQ and MASTER bits sets the TWI operational mode.

CT1, CT0

These two bits set the Timer I preload value at every SCL transition. This allows the user to optimize the TWI bus timing for a given oscillator speed. These bits are cleared by reset

CT1, CT0 Values			
CT1,CT0	OSC/12 Count	Max Osc Frequency	Timeout Period
1 0	7	16.8	1023 cycles
0 1	6	14.4	1022 cycles
0 0	5	12.0	1021 cycles
1 1	4	9.6	1020 cycles

TWI Operating Modes with TIRUN

The control of Timer I is a function of the current operating mode of the TWI hardware.

When no mode is selected, TIRUN is an enable that allows Timer I to be a free-running timer

If any mode is selected, then the bottom three bits of Timer I always run, so as to provide timing information for proper TWI operation. The TIRUN bit then enables the operation of the upper Timer I bits which check for the TWI timeout conditions.

TWI Operating Modes		
SLAVEN MASTRQ MASTER	TIRUN	Mode
All 0	0	Off
All 0	1	TI is free-running timer
Any 1	0	TWI is on, but upper bits of TI do not run.
Any 1	1	Normal TWI operation

I2STA – TWI Status Register

Address = F8h
Reset value = x0100000

I2STA - TWI Status Register		
Bit	Name	Function
7	x	Not used
6	IDLE	TWI is in idle mode
5	XDATA	Transmit buffer
4	XACTV	Transmitter is active
3	MAKSTR	TWI is making a start bit
2	MAKSTP	TWI is making a stop bit
1	XSTR	TWI is making multiple start bits
0	XSTP	TWI is making multiple stop bits

This is a read-only register.

IDLE

The idle bit indicated the status of the TWI hardware. This bit is a mirror of the bit in the I2CON register.

XDATA

The content of the transmit buffer.

XACTV

This bit indicates that the transmitter is active.

MAKSTR

This bit indicates that the TWI hardware is generating a start bit.

MAKSTP

This bit indicates that the TWI hardware is generating a stop bit.

XSTR

This bit indicates that the TWI hardware is generating repeated start bits. This bit is a mirror of the bit in the I2CON register.

XSTP

This bit indicates that the TWI hardware is generating repeated stop bits. This bit is a mirror of the bit in the I2CON register.

Interrupts

The TK87C752 has six interrupt channels. These channels may be individually or collectively enabled. Unlike the classic 8051, there is only one priority level. The interrupt channels are dedicated to specific functions within the TK87C752 and are controlled by bits in the control registers.

An interrupt may be generated by software by setting the appropriate control bits.

IE – Interrupt Enable Register

Address = ABh
Reset value = 00000000

IE – Interrupt Enable Register		
Bit	Name	Function
7	EA	Enable All
6	x	
5	ETI	Enable Timer I
4	EI2	Enable TWI
3	EPWM	Enable PWM Counter
2	EX1	Enable INT1
1	ET0	Enable Timer 0
0	EX0	Enable INT0

External Interrupts

The TK87C752 has two external interrupts, which are called /INT0 and /INT1. The IT0 and IT1 bits in the TCON register determine if these interrupts are level triggered (ITn=0) or falling edge triggered (ITn=1). The interrupt bit will be reset by the interrupt hardware if it was an edge triggered interrupt. It is the programmer's responsibility to insure that the external event that generates a level triggered interrupt is satisfied and that the input is removed before the end of the interrupt service routine.

Timer 0, I Interrupts

Overflows in Timer 0 sets the TF bit in the TCON register. Overflows in Timer I set the unreadable TI bit in the I2CFG register They in turn generate the interrupt. As with the external interrupts, the interrupt hardware will reset the interrupt bit during the interrupt routine.

TWI Interrupts

A TWI interrupt will be generated if the ATN bit in the I2CON register has been set. It is the programmer’s responsibility to determine which of the 4 conditions(start, stop, data ready, or loss of arbitration) actually generated the interrupt.

PWM Interrupt

A PWM interrupt will be generated by the PWM counter overflow.

Interrupt Priorities

Interrupt priority register was removed from the TK87C752. As a result, the interrupt priorities are fixed.

Interrupt Vector Locations

The interrupt service routine starts at the following memory locations.

Interrupt Vector Locations		
Address	Priority	Source
0003h	1	IE0
000Bh	2	TF
0013h	3	IE1
001Bh	4	TI
0023H	5	TWI
0033H	6	PWM

Interrupt Response

An interrupt begins with the setting of the appropriate bit in a control register. The interrupt hardware compares the bit with the enables and priorities to determine if an interrupt request is warranted and which interrupt should be requested. This logic provides either a request for a priority 1 or a priority 0 interrupt. This logic also prepares a vector address for the interrupt service routine.

If the processor is at the end of an instruction, and if the current instruction is not a RETI, and the current instruction does not involve a write to either the IP or IE registers, and the processor is not currently servicing an interrupt of equal or higher priority, then the interrupt request will be granted, and the processor will execute the interrupt service routine. Under normal operation, the program counter is incremented immediately after an opcode fetch. This action is inhibited by the interrupt, and the program counter is frozen at the current value. The interrupt service routine then pushes the program counter onto the stack, sets an internal interrupt status bit, clears the upper byte of the program counter, and loads the lower byte with the interrupt vector. Overall, the interrupt service routine behaves as a subroutine call.

Interrupt Return

The RETI instruction should be used for a return from a subroutine. This instruction is the same as a RET instruction, except that it clears the internal interrupt status bit, and thus enables future interrupts.

Power Management

The TK87C752 provides for the two standard power management modes and for the POR status bit.

PCON – Power Control Register

Address = 87h
Reset value = 00000000b

Power Control (PCON)		
Bit	Name	Function
7	x	Not used
6	x	Not used
5	x	Not used
4	POF	Power On Flag
3	GF1	User Flag 1
2	GF0	User Flag 0
1	PD	Powerdown
0	IDL	Idle

Idle Mode

The idle mode is entered by setting the IDLE bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will leave idle when either an interrupt or a reset occurs.

Power Down Mode

When the PD bit of the PCON register is set, the processor enters the power down mode. During this mode all of the clocks, including the oscillator are stopped. The only way to exit power down mode is with a reset.

GF0, GF1

Bits 2 and 3 of the PCON register are user definable, general purpose flags.

POR Flag

Bit 4 of the PCON register contains a power-on- flag. This bit is set when VDD has been applied to the part. If it is subsequently reset by software, it can be used to determine if a reset is a warm boot or a cold boot.

Stopping the Clock

The clock for the TK87C752 may be stopped externally at any time and in any state. It may then be resumed at any time without interference with the processor operation. The only consideration is that the external clock stopping logic should not cause glitches on the clock input.

Pulse Width Modulation Output (P0.4)

The TK87C752 contains an 8 bit PWM whose output is on pin P0.4. The PWM consists of an 8-bit prescaler, followed by a duty cycle generator.

PWMP Register

There is an 8-bit prescaler that operates off of the internal 8051 clock, and provides the clock for the duty cycle generator. The prescaler is programmed by the contents of the PWMP register, located at 8Fh. The prescaler provides a divide-by- (1+PWMP) function from the internal clock (XTAL / 2).

PWC Register

The PWC register, at 8Eh, sets the duty cycle of the output signal.

Loading the register with a 0 keeps the output continuously high. Loading it with a FFh keeps the output continuously low. Loading it with a 40h produces an output waveform with a 75% duty cycle.

The counter counts from 0 to 254. At 0, the count is set low. When the count is equal to the contents of the PWC register, the output goes high, and remains high for the rest of the count.

Enable Register

Setting bit 0 in the PWENA register, at FEh, enables the PWN circuitry. When the PWE bit is enables, pin P0.4 changes so that the output is a strong push-pull output.

Output Frequency

The PWM output frequency is given by

Fpwm = Fosc / (2 * 255 * (1 + PWMP))

This provides frequencies from 92 Hz to 23.5 KHz with a oscillator frequency of 12 MHz.

The PWM function is disabled during RESET and remains disabled after reset is removed until re-enabled by software. The PWM output is high during power down and idle. The counter is disabled during idle.

An interrupt will be asserted upon PWM counter overflow if the interrupt is not masked off.

The PWM output is an alternative function of P0.4. In order to use this port as a bidirectional I/O port, the PWM output must be disabled by clearing the enable/disable bit in PWENA. In this case, the PWM subsystem can be used as an interval timer by enabling the PWM interrupt.

PWENA – PWM Enable Register

Address = FEh
Reset value = xxxxxxx0b

PWM Enable (PWENA)		
Bit	Name	Function
7	x	Not used
6	x	Not used
5	x	Not used
4	x	Not used
3	x	Not used
2	x	Not used
1	x	Not used
0	PWE	Pulse Width Enable

Memory

RAM

The 87C752 contains 128 bytes of RAM, located from 00h to 7Fh in the SFR address space.

Flash

The 87C752 contains 64K bytes of Flash memory, located from 0000h to FFFFh in the program address space.

A/D Converter

The analog circuitry in the TK87C752 consists of an 8-bit ADC with a 5-input analog multiplexer. The conversion takes 480 crystal clocks (40 internal machine cycles @ 12 clocks per cycle.

The A/D converter is controlled by the ADCON control register. ADCON register bits 0-2 control the analog multiplexer which selects which input channel is being measured.

ADCON – ADC Control Register

Address = A0h
Reset value = 11000000b

ADC Control Register (ADCON)		
Bit	Name	Function
7	x	Not used
6	x	Not used
5	ENADC	1 = enable ADC
4	ADCI	ADC Interrupt Flag
3	ADCS	ADC Start
2	AADR2	Analog Input Select
1	AADR1	Analog Input Select
0	AADR0	Analog Input Select

ADCI ADC Interrupt Flag.

This flag is set on the completion of an ADC conversion. It is cleared by reading the ADC Data register at address 84h. This is a read-only bit.

ADCS ADC Start Bit

Writing a 1 to this bit starts an ADC conversion. The bit is reset at the end of the conversion. Writing to the ADCS bit during a conversion will have no effect. Writing a 0 to this bit will also have no effect.

ADDR2, ADDR1, ADDR0 Address Selection Bits

ADDR2	ADDR1	ADDR0	Channel
0	0	0	P1.0
0	0	1	P1.1
0	1	0	P1.2
0	1	1	P1.3
1	0	0	P1.4

At the completion of the ADC conversion, ADCI is set, and the result is stored in the special function register ADAT (84h).

When the ENADC bit is a 0, the analog input pins ADC0-ADC4 may be used as digital inputs and outputs. When the ENADC bit is enabled, the analog input channel that is selected by the ADDR2-ADDR0 bits cannot be used as a digital input. This bit will always be a 1 when read. The unselected A/D inputs may be used as digital inputs. Unselected analog inputs will be floating and may not be used as digital outputs.

The A/D reference inputs on the 87C752 are tied together to the analog supply pins AVCC and AVSS. As a result, the reference voltage on the A/D cannot be varied separately from the analog supply pins. AVSS must be connected to ground and AVCC must be connected to a supply voltage between 4.5V and 5.5V. A/D measurements may be made in the range of 4.5V to 5.5V.

The AVSS pin must be kept at ground, and AVDD must be in the range of 4.5 to 5.5 volts. Increasing the voltage on the A/D ground reference above 0V or reducing the voltage on the positive A/D reference below 4.5V can damage the part.

Programming the Flash

The original NXP parts used an EPROM technology, and required a high voltage to program the parts. Using a Tekmos part in a programmer designed for the original NXP parts will damage the Tekmos part, and should not be done.

Tekmos is working with external programmer vendors to support the Tekmos part. Until this support is available, Tekmos will program customer parts at no charge. All that is needed is the original hex file.

Electrical Specifications

Maximum Ratings

Characteristics		Symbol	Min	Max	Unit
Supply Voltage		Vdd	-0.5	6	V
Input Voltage		Vin	Vss – 0.3	Vdd + 0.3	V
Current Drain per Pin		Imax		15	mA
Operating Temperature Range	Industrial	Tai	-40	85	ºC
Storage Temperature range		Tstg	-55	+150	ºC

DC Electrical Specifications (Vdd = 5.0 V +/- 10%, Vss = 0 V, Ta = -40ºC to +85ºC)

Characteristics	Condition	Symbol	Min	Max	Unit
Input high level (Ports 0, 1, 2, 3, /EA)		V_{IH}	2.0	Vdd	V
Input high level (X1, RST)		V_{IH1}	2.0	Vdd	V
Input low level		V_{IL}	0.0	0.8	V
Output high level	Ioh = 2 mA	V_{OH}	2.4	Vdd	V
Output high level	Ioh = 4 mA	V_{OH1}	2.4	Vdd	V
Output High Level P0.4, PWM Enabled					
Output low level	Iol = 2 mA	V_{OL}	0	0.4	V
Output low level	Iol = 4 mA	V_{OL1}	0	0.4	V
Input current (Ports 1, 2, 3)	V_{IN} = 0.4 V	I_{LI}	-10	10	uA
Logical 1 to 0 transition current (Ports 1, 2, 3)	Note 2	I_{TL}	-10	10	uA
Input Leakage current (Port 0)		I_L	-10	10	uA
Supply current, Active mode,	X1 = 12 MHz	I_{CCA}		20	mA
Internal Reset Pull-Down Resistor	Vin = 0V	R_{RST}	-10	10	uA
Pin Capacitance	Cio	C_{IO}		10	uA
Power down current	Note 3	I_{PD}		TBD	uA
Idle Mode Current	Note 4	I_{IDLE}		TBD	mA
Supply Current	Note 5	I_{DD}		TBD	mA
Analog Supply Voltage		AV_{DD}	4.5	5.5	V
Analog Operating Supply Current		AI_{DD}		3	mA
Analog Input Voltage		AV_{IN}			
Analog Input Capacitance		CIA			
Sampling Time		tADS			
Conversion Time		tADC			
Resolution		R			
Relative Accuracy		ERA			
Zero Scale Offset		OS_e			
Full Scale Gain Error		G_e			
Channel to Channel Matching		M_{CTC}			
Crosstalk		C_T			

Notes For DC Characteristics:

1. The output low current (Iol) must be externally limited as follows:

Maximum Iol per pin	10 mA
Maximum Iol per 8-bit port	26 mA
Maximum total Iol	67 ma

Exceeding these limits will cause current induced voltage drops in internal ground busses. This in turn will cause Vol to rise, and possible exceed the specifications.

2. Ports 1 and 3 source a transition current when a pin is pulled from a 1 to a 0. This current reaches a peak value around 2 volts.
3. The power down current is measured with port 0 = Vdd, ports 1 and 3 disconnected, RST = 0v, and X1 and X2 disconnected.
4. The idle mode current is measured with port 0 = Vdd, ports 1 and 3 disconnected, RST = 0v, X2 disconnected, and X1 driven by a 12 MHz clock with 5 ns rise and fall times.
5. The supply current is measured with port 0 = Vdd, ports 1 and 3 disconnected, RST = 0v, X2 disconnected, and X1 driven by a 12 MHz clock with 5 ns rise and fall times.

AC Electrical Specifications (Vdd = 5.0 V +/- 10%, Vss = 0 V, Ta = 0ºC to +70ºC)

Characteristics	Symbol	Min	Max	Unit
Oscillator Frequency	$1/T_{CLCL}$	3.5	16	MHz
External Clock High Time	T_{CH}	20		ns
External Clock Low Time	T_{CL}	20		ns
External Clock Rise Time	T_{CR}		20	ns
External Clock Fall Time	T_{CF}		20	ns

Ordering Information

Reference Number	Ordering Number	Temperature	Package	Frequency	Replaces
TK87C752-5N28-Pxxx	TK7858P	-40 to +85	Plastic 28.6 DIP	3.5 to 16 MHz	S87C752-5N28
TK87C752-5A28-Pxxx	TK7858L	-40 to +85	Plastic 28 LGA	3.5 to 16 MHz	S87C752-5A28

Pxxx is the programming code. Tekmos will provide a unique programming code for each customer program.
Packages are fully RoHS compliant.
Note: The NXP -4 parts have been replaced by the higher performance -5 parts.

Contact Information

The TK87C752 series may be ordered directly from Tekmos

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Revision History

Date	Revision	Description
1/19/09	1.0	Initial release
1/26/09	1.1	Correct errors in interrupt enables, fix typos
9/21/17	2.0	Convert to flash part, add ADC description, correct ordering information
05/14/2024	2.1	Added ordering number to ordering information table