Features

- Static 186 CPU core.
- Idle and Powerdown Modes
- Clock Generator
- 2 Serial Channels with Independent Baud Rate Generators and DMA support
- 3 Programmable 16-Bit Timers
- 4 DMA Channels
- 10 Programmable Chip Selects with Programmable Wait State Generators
- 22 Multiplexed I/O Port Pins
- 2 8259A Compatible Programmable Interrupt Controllers
- 32-Bit Watchdog Timer
- Memory Refresh Generator
- High Impedance Test Mode (ONCE)
- Power Management Unit
- On-Chip Oscillator
- 16 MHz High Speed Operation
- 1 MB Memory Address Capability
- 64 KB I/O Address Capability
- High Speed Operation
  - 25 MHz @ 5 V
  - 16 MHz @ 3 V
- 100 Pin EIAJ Quad Flat Pack
- System Level testing support
- Extended Temperature Range (-40C to +85C)
- Direct replacement for Intel 80C186EC / 80C188EC microprocessors

General Description

The TK80C186EC and the TK80C188EC are based on the same die. Unless otherwise noted, discussions of the TK80C186EC can be applied to both parts.

The TK80C186EC is an enhancement of the original 80C186EA and EB microprocessors. It offers new features while remaining object code compatible with the original EA series of processors.

The TK80C186EC will work correctly at either 3 or 5 volts. The original Intel parts were sorted by minimum operating voltage to select the parts for the “L” series. With today’s improved process control, it is possible for all Tekmos parts to operate at both 3 and 5 volts. Orders for the “L” series will be filled with “C” parts.

The small feature sizes (0.35u) used in the TK80C186EC result in a significant power reduction as compared to the original devices. This is enhanced through use of the Idle and Powerdown modes. These modes stop portions of, or all of the internal clocks to achieve the power savings.

The TK80C186EC integrates commonly used system peripherals with the 186 CPU core to save space and reduce overall power consumption. A programmable interrupt controller supports and prioritizes 128 interrupts from internal, external, and software sources. The TK80C186EC also contains three programmable timer / counters and two serial channels.

Figure 1 shows the block diagram for the TK80C186EC / TK80C188EC.

Block Diagram

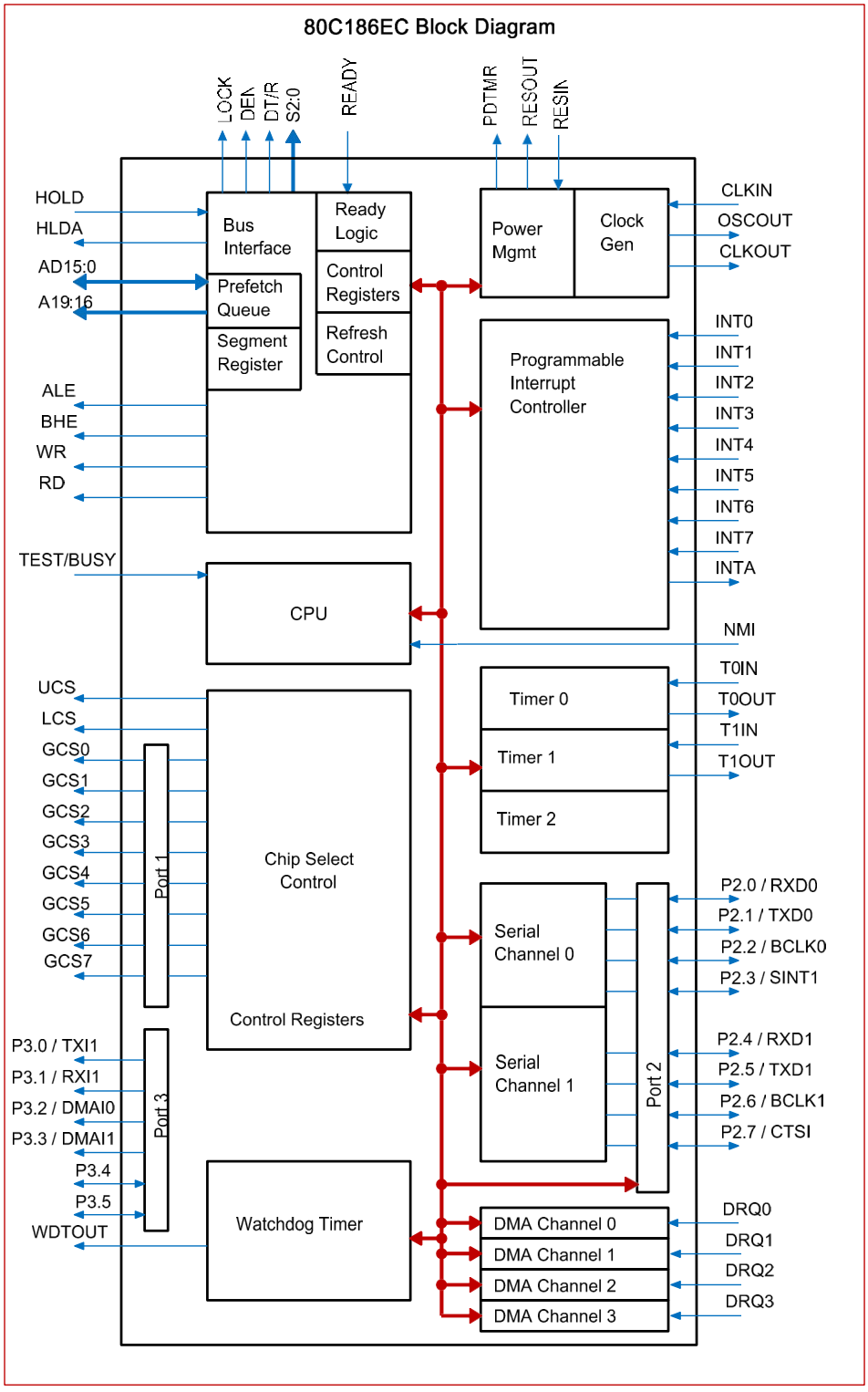

Figure 1 - TK80C186EC / TK80C188EC Block Diagram

TK80C186EC Core Architecture

Bus Interface Unit

The bus interface unit generates the local bus control signals. It uses a HOLD / HLDA protocol to share the bus with other bus masters.

The Bus Interface Unit generates the 20 bit address, read strobe, write strobe, data, and bus cycle status information. It also reads data off of the local bus during a read operation. The READY pin optionally extends the bus cycle beyond the minimum 4 clocks.

The Bus Interface Unit also generates the DEN and DT/R control signals for external transceiver chips. This allows for the buffering of the multiplexed address / data bus.

Clock Generator

The TK80C186EC contains a clock generator that supports both internal and external clock generation. It consists of a crystal oscillator, a divide-by-two circuit, and clock gating circuitry to support the power-down and idle modes.

The clock generator can be used with either a crystal or it can be driven directly from an external clock source. Figure 2 shows the connections for both cases.

The crystal or clock frequency must be twice the desired operating frequency due to the divide-by-two circuit. This produces a 50% duty cycle on the internal clock, and makes the processor performance independent of duty cycle variations present on the input clock. The internal clock is available on the CLKOUT pin. All AC timings are referenced to the CLKOUT pin.

TK80C186EC Peripherals

The TK80C186EC contains a number of integrated peripherals. These flexible peripherals are integrated with each other to provide a solution to most processor applications.

The TK80C186EC contains the following peripherals:

- 2 cascaded 8258A Interrupt Controllers
- 3 Channel Timer / Counter
- 2 Channel Serial Controller
- 4 Channel DMA
- 10 Output Chip Select Controller
- DRAM Refresh Controller
- 3 8-bit parallel ports
- Power Management Logic

All of the peripheral control registers are contained within a 128x16 Peripheral Control Block (PCB). The PCB can be relocated to either memory or I/O space on any 256 byte address boundary.

Figure 3 shows the register assignments in the PCB.

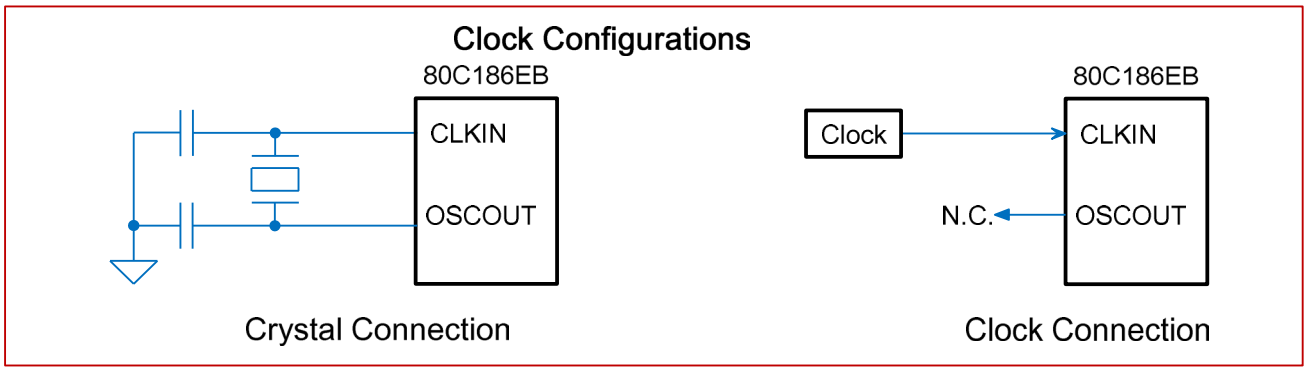

Figure 2 – Clock Configurations

PCB Register Assignments							
PCB	**Function**	**PCB**	**Function**	**PCB**	**Function**	**PCB**	**Function**
00	Master PIC Port 0	40	Timer 2 Count	80	GCS0 Start	C0	DMA0 SL
02	Master PIC Port 1	42	Timer 2 Compare	82	GCS0 Stop	C2	DMA0 SH
04	Slave PIC Port 0	44	Reserved	84	GCS1 Start	C4	DMA0 DL
06	Slave PIC Port 1	46	Timer 2 Control	86	GCS1 Stop	C6	DMA0 DH
08	Reserved	48	Port 3 Direction	88	GCS2 Start	C8	DMA0 Cnt.
0A	SCU Int. Req. Ltch.	4A	Port 3 Pin	8A	GCS2 Stop	CA	DMA0 Ctrl.
0C	DMA Int. Req. Ltch.	4C	Port 3 Control	8C	GCS3 Start	CC	DMA Priorit
0E	TCU Int. Req. Ltch.	4E	Port 3 Latch	8E	GCS3 Stop	CE	DMA Halt
10	Reserved	50	Port 1 Direction	90	GCS4 Start	D0	DMA1 SL
12	Reserved	52	Port 1 Pin	92	GCS4 Stop	D2	DMA1 SH
14	Reserved	54	Port 1 Control	94	GCS5 Start	D4	DMA1 DL
16	Reserved	56	Port 1 Latch	96	GCS5 Stop	D6	DMA1 DH
18	Reserved	58	Port 2 Direction	98	GCS6 Start	D8	DMA1 Cnt.
1A	Reserved	5A	Port 2 Pin	9A	GCS6 Stop	DA	DMA1 Ctrl.
1C	Reserved	5C	Port 2 Control	9C	GCS7 Start	DC	Reserved
1E	Reserved	5E	Port 2 Latch	9E	GCS7 Stop	DE	Reserved
20	WDT Reload High	60	Serial 0 Baud	A0	LCS Start	E0	DMA2 SL
22	WDT Reload Low	62	Serial 0 Count	A2	LCS Stop	E2	DMA2 SH
24	WDT Count High	64	Serial 0 Control	A4	UCS Start	E4	DMA2 DL
26	WDT Count Low	66	Serial 0 Status	A6	UCS Stop	E6	DMA2 DH
28	WDT Clear	68	Serial 0 RBUF	A8	Relocation	E8	DMA2 Cnt.
2A	WDT Disable	6A	Serial 0 TBUF	AA	Reserved	EA	DMA2 Ctrl.
2C	Reserved	6C	Reserved	AC	Reserved	EC	Reserved
2E	Reserved	6E	Reserved	AE	Reserved	EE	Reserved
30	Timer 0 Count	70	Serial 1 Baud	B0	Refresh Base	F0	DMA3 SL
32	Timer 0 Compare A	72	Serial 1 Count	B2	Refresh Time	F2	DMA3 SH
34	Timer 0 Compare B	74	Serial 1 Control	B4	Refresh Ctrl.	F4	DMA3 DL
36	Timer 0 Control	76	Serial 1 Status	B6	Refresh Addr.	F6	DMA3 DH
38	Timer 1 Count	78	Serial 1 RBUF	B8	Power Control	F8	DMA3 Cnt.
3A	Timer 1 Compare A	7A	Serial 1 TBUF	BA	Reserved	FA	DMA3 Ctrl.
3C	Timer 1 Compare B	7C	Reserved	BC	Step ID	FC	Reserved
3E	Timer 1 Control	7E	Reserved	BE	Powersave	FE	Reserved

Figure 3 – PCB Register Assignments While in Master Mode

Interrupt Controller

The TK80C186EC contains 2 8259A Programmable Interrupt Controllers (PIC). They are configured in a master / slave arraignment. INT0:6 are connected to the master, and INT7 is connected to the slave.

There are 11 internal interrupt sources. 4 from the serial controller, 4 from the DMA controller, and 3 from the timer / counter.

The NMI interrupt pin is directly connected to the CPU.

Serial Controller

The Serial controller contains two independent channels. Each channel has its own baud rate generator, or may be clocked through an external baud rate source.

Each serial channel has one synchronous mode and 4 asynchronous modes. These modes support various data lengths and parity options.

In addition, the serial channels support a multiprocessor protocol for devices connected to a common serial bus.

Both Serial channels are supported by the DMA unit, providing block reception and transmission without CPU intervention.

DMA Unit

The DMA unit contains two modules, each of which has two channels. DMA can occur in any combination between memory and I/O. A DMA request can be generated externally, internally, or though software.

The DMA works with bytes only, and each byte requires two bus cycles to complete.

Timer / Counter

The timer / counter contains 3 16-bit timers. Two of them may be connected to external pins for clocking or control. The third timer is clocked internally, but may be used to provide a clock source to the other two timers.

The timers may be programmed to meet the needs of many applications, In addition to keeping track of the passage of time, they may also count or time external events, or generate non-repetitive waveforms.

Chip Select Controller

The Chip Select Controller generates up to 10 programmable chip selects for accessing both memories and peripherals. Each chip select can also be programmed to terminate a bus cycle independently of the state of the READY pin. The chip selects are available for all bus cycles, independent of the internal source (CPU or refresh).

Refresh Controller

The refresh controller supports the use of DRAMs by generating periodic read cycles of consecutive 12-bit addresses. The delay between the cycles is programmable up to 512 clocks. The high order address lines are also programmable to support refresh cycles on any 8K memory block.

Power Management

The power management logic provides two modes to control the power consumption. These are:

- Idle Mode
- Power Down Mode

The idle mode stops the CPU and Bus clocks, while allowing the peripheral clocks to continue to run. This reduces overall power while allowing the peripherals to remain active and to awaken the processor as necessary.

The power down mode stops the oscillator and all internal clocks. All registers maintain their values as long as Vdd is present. Current is reduced to leakage values.

I/O Ports

The TK80C186EC has 2 8-bit I/O ports and one 6-bit port. The pins are multiplexed with the control signals for the other internal peripherals.

Watchdog Timer

The watchdog timer is a 32 bit counter that can be reset by software. Should the watchdog timer time-out, the /WDTOUT pin will be pulled low for 4 clock cycles. This may be ANDed with the reset signal to reset the device.

80C187 Interface (TK80C186EC Only)

The TK80C186EC does not support the interface to the external 80C187 math coprocessor. The interface pins are labeled for convenience.

Once Test Mode

The ONCE mode can be activated by forcing the A19 pin low during a processor reset. This in turn forces all input and output pins into a high-impedance state.

Pin Descriptions

VCC - Supply

Positive Power Supply

GND - Supply

Ground

CLKIN - Input

Clock Input. CLKIN is 2X the internal clock speed. CLKIN may be used with OSCOUT to create a crystal oscillator.

OSCOUT - Output

The OSCOUT pin is used with CLKIN to create a crystal oscillator. The OSCOUT pin should be left unconnected when CLKIN is directly driven.

CLKOUT - Output

CLKOUT is a divide-by-two of the CLKIN pin, triggering on every CLKIN falling edge. It is used as the timing references for all processor AC specifications.

RESIN* – Input

RESIN (Reset In) causes the processor to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the processor begins fetching opcodes at memory location 0FFFF0H.

RESOUT – Output

RESOUT (Reset Output) indicates the processor is currently in the reset state. RESOUT will remain active as long as RESIN remains active

PDTMR – Bidirectional

The PDTMR (Power-Down Timer) determines the amount of time the processor waits after an exit from power down before resuming normal operation. This pin is normally connected to an external capacitor. The duration of time required will depend on the startup characteristics of the crystal oscillator.

NMI – Input

The NMI (Non-Maskable Interrupt) pin causes a Type 2 interrupt to be serviced by the CPU. NMI is latched internally.

TEST* / BUSY – Input

The TEST* / BUSY pin is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (low). This pin also receives the BUSY signal from the 80C187 Numerics Coprocessor.

AD15 – AD0 – Bidirectional

These pins provide a multiplexed Address and Data bus. During the address phase of the bus cycle, address bits 0 through 15 are presented on the bus and can be latched using ALE. 8- or 16-bit data information is transferred during the data phase of the bus cycle. In the -188 versions, pins AD8 to AD15 provide valid address information for the entire cycle.

Pins AD15 to AD13 drive the CAS2:0 slave address information from the 82C59 during interrupt acknowledge cycles.

A19 / ONCE* - A16 – Output

These pins provide multiplexed Address during the address phase of the bus cycle. Address bits 16 through 19 are presented on these pins and can be latched using ALE. These pins are driven to a logic 0 during the data phase of the bus cycle.

Forcing A19 low during reset triggers the ONCE mode.

S2, S1, S0 – Output

Bus cycle Status are encoded on these pins to provide bus transaction information. S2-S0 are encoded as follows:

S2	S1	S0	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Processor HALT
1	0	0	Queue Instruction Fetch
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive (no bus activity)

ALE – Output

Address Latch Enable output is used to latch address information during the address phase of the bus cycle.

BHE* – Output

Byte High Enable output to indicate that the bus cycle in progress is transferring data over the upper half of the data bus. BHE and A0 have the following logical encoding:

A0	BHE	Encoding (80C186EC Only)
0	0	Word Transfer
0	1	Even Byte Transfer
1	0	Odd Byte Transfer
1	1	Refresh Operation

On the 80C188EC/80L188EC, RFSH is asserted low to indicate a Refresh bus cycle.

RD* – Output

The RD* (Read) output signals that the accessed memory or I/O device must drive data information onto the data bus.

WR* – Output

The WR* (Write) output signals that data available on the data bus are to be written into the accessed memory or I/O device.

READY – Input

READY is an input to signal for the end of a bus cycle. READY must be active to terminate any processor bus cycle, unless it is ignored due to the programming of the Chip Select Unit.

DEN* – Output

The DEN* (Data Enable) output controls the enable of bidirectional transceivers in a buffered. DEN* is active only when data is to be transferred on the bus.

DT/R – Output

The DT* / R (Data Transmit/Receive) output controls the direction of a bidirectional buffer in a buffered system. DT/R is only available on the PLCC 84 package.

LOCK* – Output

LOCK* output indicates that the bus cycle in progress is not to be interrupted. The processor will not service other bus requests (such as HOLD) while LOCK* is active. This pin is configured as a weakly held high input while RESIN is active and must not be driven low.

HOLD – Input

HOLD request input to signal that an external bus master wishes to gain control of the local bus. The processor will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.

HLDA – Output

The HLDA (Hold Acknowledge) output indicates that the processor has relinquished control of the local bus. When HLDA is asserted, the processor has floated its data bus and control signals allowing another bus master to drive the signals directly.

NCS* – NC

The NCS* (Numeric Coprocessor Select) pin accesses the Numeric Coprocessor. This pin is not supported in the Tekmos design.

ERROR* – NC

The ERROR pin indicates that the last numeric coprocessor operation resulted in an exception condition. This pin is not supported in the Tekmos design.

PEREQ – NC

The PEREQ (Coprocessor Request) input signals that a data transfer between the external coprocessor and memory is pending. This pin is not supported in the Tekmos design.

UCS* – Output

Upper Chip Select will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. After reset, UCS* is configured to be active for memory accesses between 0FFC00H and 0FFFFFH. During a processor reset, UCS* and LCS* are used to enable ONCE Mode.

LCS* – Output

Lower Chip Select will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. LCS is inactive after a reset.

P1.0 – P1.7 / GCS0* - GCS7*– Output

These pins provide a multiplexed function. If enabled, each pin can provide a generic chip select function. When not programmed as a chip select, each pin can function as a general purpose output port. As an output port, each pin can be read internally.

T0OUT, T1OUT – Output

The Timer Output pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected.

T0IN, T1IN – Input

The Timer Inputs are used either as clock or control signals, depending on the timer mode selected.

INT0 – INT7 – Input

Maskable interrupt inputs will cause a vector to a specific Type interrupt routine. The INT0 – INT6 pins can be used as interrupt cascade inputs from external 82C59A slave devices.

P3.5 / P3.4 – Bidirectional

These pins are bidirectional, open drain, general purpose port pins.

P3.3 / DMAI1, P3.2 / DMAI0 – Output

The DMA Interrupt outputs go active when a DMA channel has completed a transfer. These signals are multiplexed with the Port 3 pins.

P3.1 / TXI1 – Output

The transmit interrupt goes active when serial channel 1 has completed transmission. This signal is multiplexed with P3.1.

P3.0 / RXI1 – Output

The receive interrupt goes active when serial channel 1 has received a character. This signal is multiplexed with P3.0.

WDTOUT* – Output

The watchdog timer output is driven low for 4 clocks when the watchdog timer reaches zero.

P2.7 / CTS1*, P2.3 / CTS0* - Bidirectional

The Clear-To-Send function controls transmission on their respective serial channel. These pins are multiplexed with the Port 2 pins.

P2.6 / BCLK1, P2.2 / BCLK0 - Bidirectional

The baud clock pins provide an alternate baud clock source for the serial channels. The baud clock frequency cannot exceed half of the processor operating frequency. These pins are multiplexed with the Port 2 pins.

P2.5 / TDX1, P2.1 / TXD0 – Bidirectional

These pins provide the Transmit Data for the serial channels. When operating in Mode 0, these pins provide the clock for the synchronous data on the RXD pins. These pins are multiplexed with the Port 2 pins.

P2.4 / RXD1, P2.0 / RXD0 – Bidirectional

These pins are the receive data for the serial channels. In mode 0, these pins become bidirectional. These pins are multiplexed with the Port 2 pins.

DRQ3:0 – Input

These pins are used to request a DMA transfer.

Reset Operation

Basic Operation

The reset pin is synchronized internally before it is applied to the rest of the circuit. This means that the clocks must be operating while RESIN* is low to insure correct initialization of the device.

Cold Reset

It is important to insure that RESIN* remain active until the clocks have stabilized, If a RC reset circuit is used, the RC time constant must be longer than the power supply rise time.

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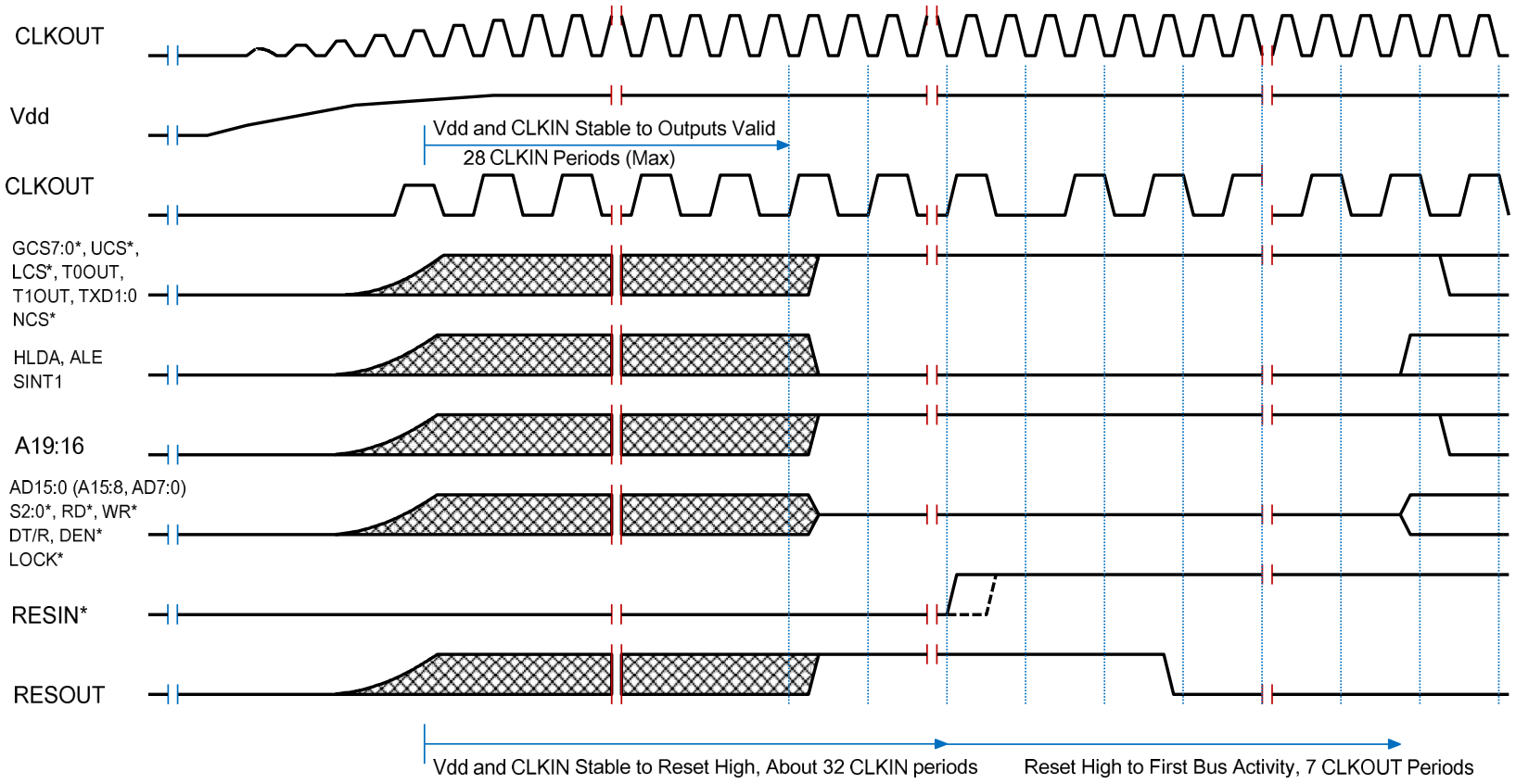
Warm Reset
RESIN* must be remain low for four CLKOUT periods to take effect. A reset will terminate all activity and bus cycles.

Solderability

The Tekmos TK80C186EC used a 100% matte tin finish on the leads. We recommend a solder profile compatible with the JEDEC-STD-20.1D. We suggest that the maximum temperature during soldering not exceed 245C.

Cold Reset Waveforms



Note:
CLKOUT synchronization occurs on the rising edge of RESIN*. If RESIN* is sampled high while CLKOUT is high (solid line), then CLKOUT will remain low for two CLKIN periods. If RESIN* is sampled high while CLKOUT is low (dashed line), then CLKOUT will not be affected.
Pin names in parentheses apply to 80C188EB.

Pinout

PQFP 100	80C186	80C188
1	DRQ0	
2	DRQ1	
3	DRQ2	
4	DRQ3	
5	T0OUT	
6	T0IN	
7	T1OUT	
8	T1IN	
9	CLKOUT	
10	RESOUT	
11	RESIN_n	
12	PDTMR	
13	CLKIN	
14	OSCOUT	
15	VSS	
16	VDD	
17	VDD	
18	VSS	
19	P2.0 / RXD0	
20	P2.1 / TXD0	
21	P2.2 / BCLK0	
22	P2.3 / CTS0_n	
23	P2.4 / RXD1	
24	P2.5 / TXD1	
25	P2.6 / BCLK1	
26	P2.7 / CTS1_n	
27	P3.0 / RXI1	
28	P3.1 / TXI1	
29	P3.2 / DMAI0	
30	P3.3 / DMAI1	
31	P3.4	
32	P3.5	
33	INT0	
34	INT1	
35	INT2	
36	INT3	
37	INTA_n	
38	NCS_N	NC
39	WDTOUT_n	
40	VSS	
41	VDD	
42	VSS	
43	INT4	
44	INT5	
45	INT6	
46	INT7	
47	HOLD	
48	HLDA	
49	DT/R_n	
50	DEN_n	

PQFP 100	80C186	80C188
51	LOCK_n	
52	WR_n	
53	RD_n	
54	BHE_n	RFSH_n
55	ALE	
56	AD15	A15
57	AD14	A14
58	AD13	A13
59	AD12	A12
60	AD11	A11
61	AD10	A10
62	AD9	A9
63	AD8	A8
64	VSS	
65	VDD	
66	AD7	
67	AD6	
68	AD5	
69	AD4	
70	VDD	
71	VSS	
72	VDD	
73	AD3	
74	AD2	
75	AD1	
76	AD0	
77	A19 / S6 / ONCE_n	
78	A18 / S5	
79	A17 / S4	
80	A16 / S3	
81	S0_n	
82	S1_n	
83	S2_n	
84	PEREQ	VSS
85	NM1	
86	TEST_n	
87	ERROR_n	VDD
88	READY	
89	VDD	
90	VSS	
91	UCS_n	
92	LCS_n	
93	P1.7 / GCS7_n	
94	P1.6 / GCS6_n	
95	P1.5 / GCS5_n	
96	P1.4 / GCS4_n	
97	P1.3 / GCS3_n	
98	P1.2 / GCS2_n	
99	P1.1 / GCS1_n	
100	P1.0 / GCS0_n	

TQFP 100	80C186	80C188
1	DRQ3	
2	T0OUT	
3	T0IN	
4	T1OUT	
5	T1IN	
6	CLKOUT	
7	RESOUT	
8	RESIN_n	
9	PDTMR	
10	CLKIN	
11	OSCOUT	
12	VSS	
13	VDD	
14	VDD	
15	VSS	
16	P2.0 / RXD0	
17	P2.1 / TXD0	
18	P2.2 / BCLK0	
19	P2.3 / CTS0_n	
20	P2.4 / RXD1	
21	P2.5 / TXD1	
22	P2.6 / BCLK1	
23	P2.7 / CTS1_n	
24	P3.0 / RXI1	
25	P3.1 / TXI1	
26	P3.2 / DMAI0	
27	P3.3 / DMAI1	
28	P3.4	
29	P3.5	
30	INT0	
31	INT1	
32	INT2	
33	INT3	
34	INTA_n	
35	NCS_N	NC
36	WDTOUT_n	
37	VSS	
38	VDD	
39	VSS	
40	INT4	
41	INT5	
42	INT6	
43	INT7	
44	HOLD	
45	HLDA	
46	DT/R_n	
47	DEN_n	
48	LOCK_n	
49	WR_n	
50	RD_n	

TQFP 100	80C186	80C188
51	BHE_n	RFSH_n
52	ALE	
53	AD15	A15
54	AD14	A14
55	AD13	A13
56	AD12	A12
57	AD11	A11
58	AD10	A10
59	AD9	A9
60	AD8	A8
61	VSS	
62	VDD	
63	AD7	
64	AD6	
65	AD5	
66	AD4	
67	VDD	
68	VSS	
69	VDD	
70	AD3	
71	AD2	
72	AD1	
73	AD0	
74	A19 / S6 / ONCE_n	
75	A18 / S5	
76	A17 / S4	
77	A16 / S3	
78	S0_n	
79	S1_n	
80	S2_n	
81	PEREQ	VSS
82	NM1	
83	TEST_n	
84	ERROR_n	VDD
85	READY	
86	VDD	
87	VSS	
88	UCS_n	
89	LCS_n	
90	P1.7 / GCS7_n	
91	P1.6 / GCS6_n	
92	P1.5 / GCS5_n	
93	P1.4 / GCS4_n	
94	P1.3 / GCS3_n	
95	P1.2 / GCS2_n	
96	P1.1 / GCS1_n	
97	P1.0 / GCS0_n	
98	DRQ0	
99	DRQ1	
100	DRQ2	

Electrical Specifications

Maximum Ratings

Characteristics		Symbol	Min	Max	Unit
Supply Voltage		Vdd	-0.5	5.5	V
Input Voltage		Vin	Vss – 0.3	Vdd + 0.3	V
Current Drain per Pin		I_{OL}		15	mA
Operating Temperature Range	Commercial Industrial	Tac Tai	0 -40	70 85	°C °C
Storage Temperature range		Tstg	-55	+150	°C

DC Electrical Specifications (Vdd = 5.0 V +/- 10%, Vss = 0 V, Ta = 0°C to +70°C)

Characteristics	Condition	Symbol	Min	Max	Unit
Supply Voltage		V_{DD}	4.5	5.5	V
Input Low Voltage		V_{IL}	-0.5	0.3 * Vdd	V
Input High Voltage		V_{IH}	0.7 * Vdd	5.5	V
Output Low Voltage	Iol = 3 mA	V_{OL}	0.0	0.45	V
Output High Voltage	Ioh = -2 mA	V_{OH}	Vdd - 0.5	Vdd	V
Input Hysteresis on /RESIN		V_{HYR}	0.50		V
Input Leakage Current for Pins: AD15:0, READY, HOLD, RESIN*, CLKIN, TEST*, NMI, INT7:0, T0IN, T1IN, P2.7-P2.0, P3.5-P3.0, DRQ3:0, PEREQ, ERROR*	0 < V_{IN} < V_{DD}	I_{IL1}	-15	+15	uA
Input Leakage Current for Pins: A19/ONCE*, A18:A16, LOCK*	Note 1	I_{IL3}	-0.275	-5.0	mA
Output Leakage Current	0.45 < V_{OUT} < V_{DD} Note 2	I_{OL}	-15	15	uA
Supply Current Cold (RESET) 25 MHz 20 MHz 13 MHz	 Notes 3, 7 Note 3 Note 3	I_{DD}		 125 100 70	 mA mA mA
Supply Current in Idle Mode 25 MHz 20 MHz 13 MHz	 Note 4, 7 Note 4 Note 4	I_{ID}		 92 76 50	 mA mA mA
Supply Current in Powerdown Mode 25 MHz 20 MHz 13 MHz	 Note 5, 7 Note 5 Note 5	I_{PD}		 100 100 100	 uA uA uA
Output Pin Capacitance	T_F = 1 MHz Note 6	C_{OUT}		15	pF
Input Pin Capacitance	T_F = 1 MHz	C_{IN}		15	pF

Notes:

1. RD/QSMD, /UCS, /LCS, /LOCK and /TEST/BUSY have an internal pullup that is activated during reset.
2. Output pins are floated during HOLD or ONCE mode.
3. Measured with device in reset, at worst case temperature and Vdd, and all outputs loaded.
4. Measured with the device in HALT, and IDLE Mode active
5. Measured with the device in HALT, and Powerdown Mode active
6. Output capacitance is capacitive load of a floating output pin.
7. Operating conditions for 25 MHz is 0 to 70C, Vcc = 5V +/- 10%.

AC Electrical Specifications (Vdd = 5.0 V +/- 10%, Vss = 0 V, Ta = 0°C to +70°C)

Characteristics	Note	Symbol	Min	Max	Unit
Input Clock					
CLKIN Frequency	1	T_F	0	40	MHz
CLKIN Period	1	T_C	25		ns
CLKIN High Time	1, 2	T_{CH}	10		ns
CLKIN Low Time	1, 2	T_{CL}	10		ns
CLKIN Rise Time	1, 3	T_{CR}	1	10	ns
CLKIN Fall Time	1, 3	T_{CF}	1	10	ns
Output Clock					
CLKIN to CLKOUT Delay	1, 4	T_{CD}	0	17	ns
CLKOUT Period	1	T		$2T_C$	ns
CLKOUT High Time	1	T_{PH}	(T/2) - 5	(T/2) + 5	ns
CLKOUT Low Time	1	T_{PL}	(T/2) - 5	(T/2) + 5	ns
CLKOUT Rise Time	1, 5	T_{PR}	1	6	ns
CLKOUT Fall Time	1, 5	T_{PF}	1	6	ns
Output Delays					
ALE, S2:0*, DEN*, DT/R, BHE, RFSH, LOCK, A19:16	1, 4, 6, 7	T_{CHOV1}	3	20	ns
GCS7:0*, LCS*, UCS*, RD*, WR*, WDTOUT*	1, 4, 6, 8	T_{CHOV2}	3	23	ns
BHE*, RFSH*, DEN*, LOCK*, RESOUT, HLDA, T0OUT, T1OUT	1, 4, 6	T_{CLOV1}	3	20	ns
RD*, WR*, GCS7:0*, LCS*, UCS*, AD15:0, INTA*, S2:0*	1, 4, 6	T_{CLOV2}	3	23	ns
RD*, WR*, BHE*, RFSH*, DT/R*, LOCK*, S2:0*, A19:16	1	T_{CHOF}	0	25	ns
DEN*, AD15:0	1	T_{CLOF}	0	25	ns
Inputs					
TEST, NMI, INT7:0, T1:0IN, READY, P2.0-P2.7, P3.0-P3.5	1, 9	T_{CHIS}	10		ns
TEST, NMI, INT7:0, T1:0IN, READY, P2.0-P2.7, P3.0-P3.5	1, 9	T_{CHIH}	3		ns
AD15:0, READY	1, 10	T_{CLIS}	10		ns
AD15:0, READY	1, 10	T_{CLIH}	3		ns
HOLD, RESIN*, DRQ3:0	1, 9	T_{CLIS}	10		ns
HOLD, RESIN*, DRQ3:0	1, 9	T_{CLIH}	3		ns

Notes:

1. See AC Waveforms for waveforms and definition
2. Measured at VIH for high time, VIL for low time.
3. Only required to guarantee IDD, Maximum limits are bounded by TC, TCH and TCL.
4. Specified for a 50 pF load.
5. Specified for a 50 pF load.
6. See figure for rise and fall times.
7. TCHOV1 applies to BHE*, LOCK*, and A19:A16 only after a HOLD release.
8. TCHOV2 applies to RD and WR only after a HOLD release.
9. Setup and Hold are required to guarantee recognition
10. Setup and Hold are required for proper operation.

DC Electrical Specifications (Vdd = 3.3 V +/- 10%, Vss = 0 V, Ta = 0°C to +70°C)

Characteristics	Condition	Symbol	Min	Max	Unit
Supply Voltage		V_{DD}	3.0	5.5	V
Input Low Voltage		V_{IL}	-0.5	0.3 * Vdd	V
Input High Voltage		V_{IH}	0.7 * Vdd	Vdd + 0.5	V
Output Low Voltage	Iol = 3.0 mA	V_{OL}	0.0	0.45	V
Output High Voltage	Ioh = -2 mA	V_{OH}	Vdd - 0.5	Vdd	V
Input Hysteresis on /RESIN		V_{HYR}	0.50		V
Input Leakage Current for Pins: AD15:0, READY, HOLD, RESIN*, CLKIN, TEST*, NMI, INT7:0, T0IN, T1IN, P2.7-P2.0, P3.5-P3.0, DRQ3:0	$0 < V_{IN} < V_{DD}$	I_{IL1}	-15	+15	uA
Input Leakage Current for Pins: A19/ONCE*, A18:A16, LOCK*	Note 1	I_{IL3}	-0.275	-5.0	mA
Output Leakage Current	$0.45 < V_{OUT} < V_{DD}$ Note 2	I_{OL}	-15	15	uA
Supply Current Cold (RESET, 3.3V) 16 MHz	Note 3	I_{DD}		45	mA
Supply Current in Idle Mode (3.3V) 16 MHz	Note 4	I_{ID}		35	mA
Supply Current in Powerdown (3.3V) 16 MHz	Note 5	I_{PD}		50	uA
Output Pin Capacitance	T_F = 1 MHz	C_{OUT}		15	pF
Input Pin Capacitance	T_F = 1 MHz Note 6	C_{IN}		15	pF

Notes:

1. These pins have in internal pullup active during reset.
2. Output pins are floated during HOLD or ONCE mode.
3. Measured during RESET, with worst case frequency, Vdd, and temperature, and with all outputs loaded as specified under AC Test Conditions, and all floating outputs driven to a supply.
4. Measured during HALT and IDLE mode active, with worst case frequency, Vdd, and temperature, and with all outputs loaded as specified under AC Test Conditions, and all floating outputs driven to a supply.
5. Measured during HALT and Powerdown mode active, with worst case frequency, Vdd, and temperature, and with all outputs loaded as specified under AC Test Conditions, and all floating outputs driven to a supply.
6. Output capacitance is capacitive load of a floating output pin.

AC Electrical Specifications (Vdd = 3.3 V +/- 10%, Vss = 0 V, Ta = 0°C to +70°C)

Characteristics	Note	Symbol	Min	Max	Unit
Input Clock					
CLKIN Frequency	1	T_F	0	26	MHz
CLKIN Period	1	T_C	38.5		ns
CLKIN High Time	1, 2	T_{CH}	15		ns
CLKIN Low Time	1, 2	T_{CL}	15		ns
CLKIN Rise Time	1, 3	T_{CR}	1	10	ns
CLKIN Fall Time	1, 3	T_{CF}	1	10	ns
Output Clock					
CLKIN to CLKOUT Delay	1, 4	T_{CD}	0	20	ns
CLKOUT Period	1	T		$2T_C$	ns
CLKOUT High Time	1	T_{PH}	(T/2) - 5	(T/2) + 5	ns
CLKOUT Low Time	1	T_{PL}	(T/2) - 5	(T/2) + 5	ns
CLKOUT Rise Time	1, 5	T_{PR}	1	10	ns
CLKOUT Fall Time	1, 5	T_{PF}	1	10	ns
Output Delays					
S2:0*, DT/R, BHE*, LOCK	1, 4, 6, 7	T_{CHOV1}	3	25	ns
LCS*, UCS*, DEN*, A19:16, RD*, WR*, WDTOUT*, ALE	1, 4, 6, 8	T_{CHOV2}	3	30	ns
GCS7:0*	1, 4, 6	T_{CHOV3}	3	32	ns
LOCK*, RESOUT, HLDA, T0OUT, T1OUT	1, 4, 6	T_{CLOV1}	3	25	ns
RD*, WR*, A19:16, AD15:0, INTA*, BHE*, DEN*	1, 4, 6	T_{CLOV2}	3	30	ns
GCS7:0*, LCS*, UCS*,	1, 4, 6	T_{CLOV3}	3	32	ns
S2:0*, A19:16	1, 4, 6	T_{CLOV4}	3	34	ns
RD*, WR*, BHE*, DT/R*, LOCK*, S2:0*, A19:16	1	T_{CHOF}	0	28	ns
DEN*, AD15:0	1	T_{CLOF}	0	32	ns
Inputs					
TEST, NMI, INT7:0, T1:0IN, READY	1, 9	T_{CHIS}	15		ns
TEST, NMI, INT7:0, T1:0IN, READY	1, 9	T_{CHIH}	3		ns
AD15:0, READY	1, 10	T_{CLIS}	15		ns
AD15:0, READY	1, 10	T_{CLIH}	3		ns
HOLD, RESIN*, DRQ3:0	1, 9	T_{CLIS}	15		ns
HOLD, RESIN*, DRQ3:0	1, 9	T_{CLIH}	3		ns

Notes:

1. See AC Waveforms for waveforms and definition
2. Measured at VIH for high time, VIL for low time.
3. Only required to guarantee Idd, Maximum limits are bounded by TC, TCH and TCL.
4. Specified for 50 pF load.
5. Specified for 50 pF load.
6. See Rise and Fall time waveform.
7. TCHOV1 applies to BHE, RFSH LOCK and A19:16 only after a HOLD release
8. TCHOV2 applies to RD and WR only after a HOLD release.
9. Setup and Hold are required to guarantee recognition
10. Setup and Hold are required for proper operation

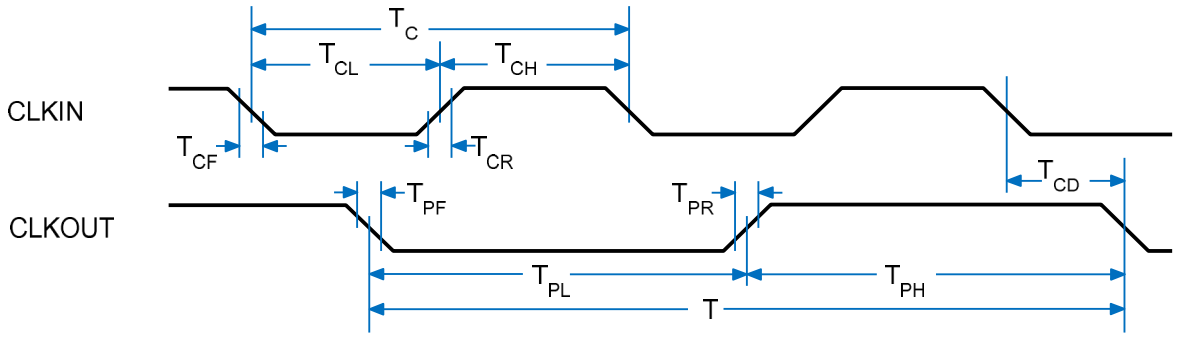
AC Electrical Specifications (Vdd = 5.0 V +/- 10%, Vss = 0 V, Ta = 0°C to +70°C)

Characteristics	Note	Symbol	Min	Max	Unit
Relative Timings					
ALE Rising to ALE Falling		T_{LHLL}	T - 15		ns
Address Valid to ALE Falling		T_{AVLL}	(T/2) - 10		ns
Chip Selects Valid to ALE Falling	1	T_{PLLL}	(T/2) - 10		ns
Address Hold form ALE Falling		T_{LLAX}	(T/2) - 10		ns
ALE Falling to WR* Falling	1	T_{LLWL}	(T/2) - 15		ns
ALE Falling to RD* Falling	1	T_{LLRL}	(T/2) - 15		ns
WR* Rising to ALE Rising	1	T_{WHLH}	(T/2) - 10		ns
Address Float to RD* Falling		T_{AFRL}	0		ns
RD* Falling to RD* Rising	2	T_{RLRH}	(2*T) - 5		ns
WR* Falling to WR* Rising	2	T_{WLWH}	(2*T) - 5		ns
RD* Rising to Address Active		T_{RHAX}	T - 15		ns
Output Data Hold after WR Rising		T_{WHDX}	T - 15		ns
WR* Rising to Chip Select Rising	1	T_{WHPH}	(T/2) - 10		ns
RD* Rising to Chip Select Rising	1	T_{RHPH}	(T/2) - 10		ns
CS* Inactive to CS* Active	1	T_{PHPL}	(T/2) - 10		ns
ONCE* Active to RESIN* Rising		T_{OVRH}	T		ns
ONCE* Hold from RESIN* Rising		T_{RHOX}	T		ns
INTA* High to Next INTA* Low during INTA cycle	4	T_{IHIL}	4T – 5		ns
INTA* Active Pulse Width	2.,4	T_{ILIH}	2T – 5		ns
CAS2:0 Setup before 2nd INTA* Pulse Low	2, 4	T_{CVIL}	8T		ns
CAS2:0 Hold after 2nd INTA* Pulse Low	2, 4	T_{ILCX}	4T		ns
Interrupt Resolution Time	3	T_{IRES}		150	ns
IR Low Time to Reset Edge Detector		T_{IRLH}	50		ns
IR Hold Time after 1st INTA* Falling	4,5	T_{IRHIF}	25		ns

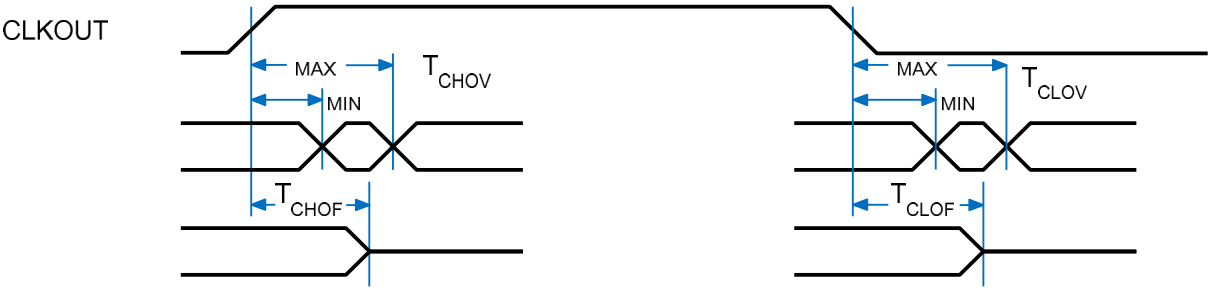
Notes:

1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Interrupt resolution time is the delay between an unmasked interrupt request going active and the interrupt output of the 8259A module going active.
4. See INTA* Cycle Waveforms
5. To guarantee that the interrupt is not spurious.

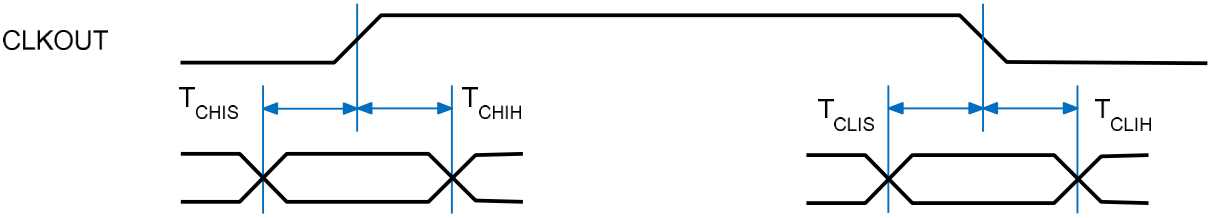
Clock Waveforms



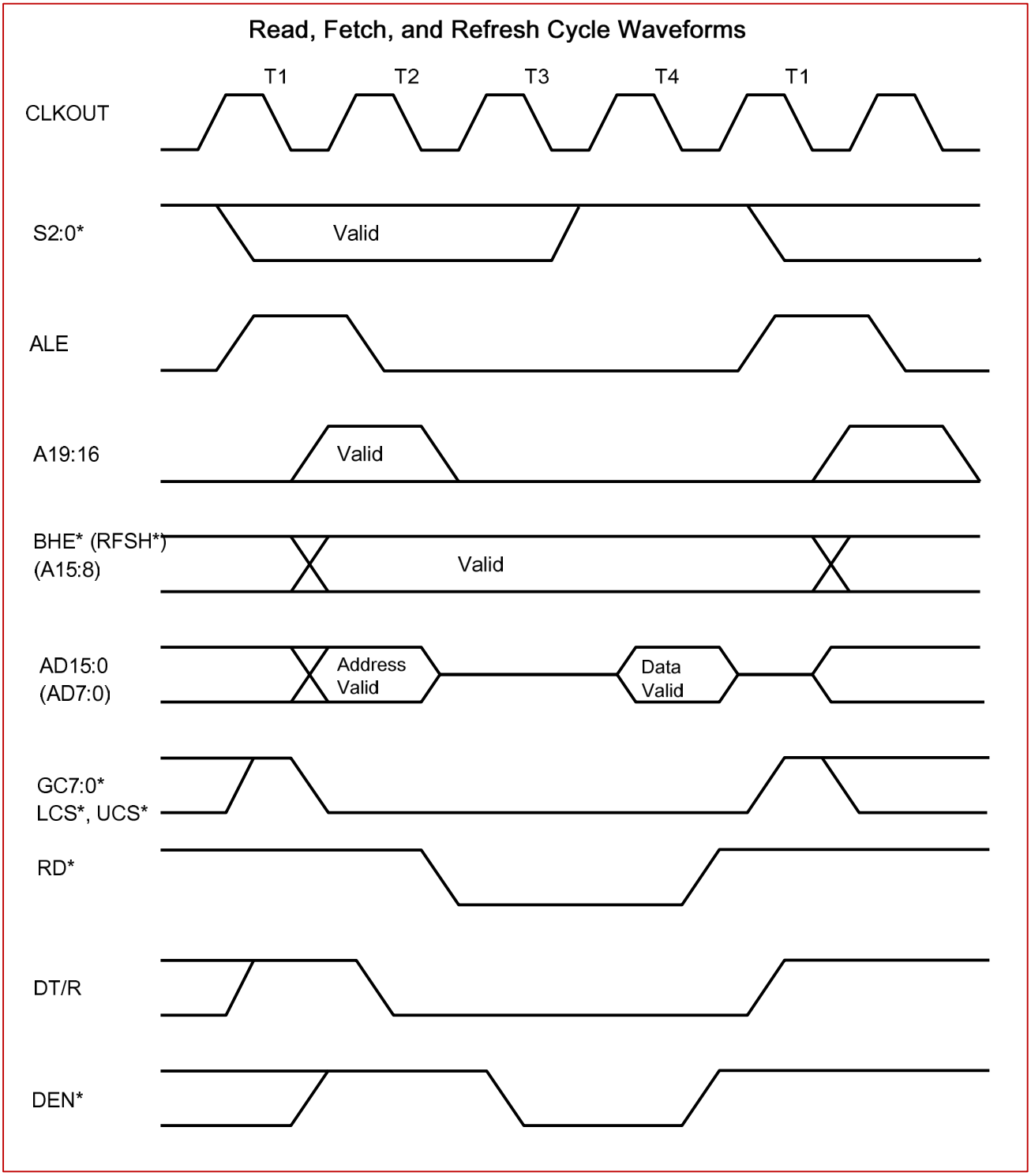
Output Delay and Float Waveforms



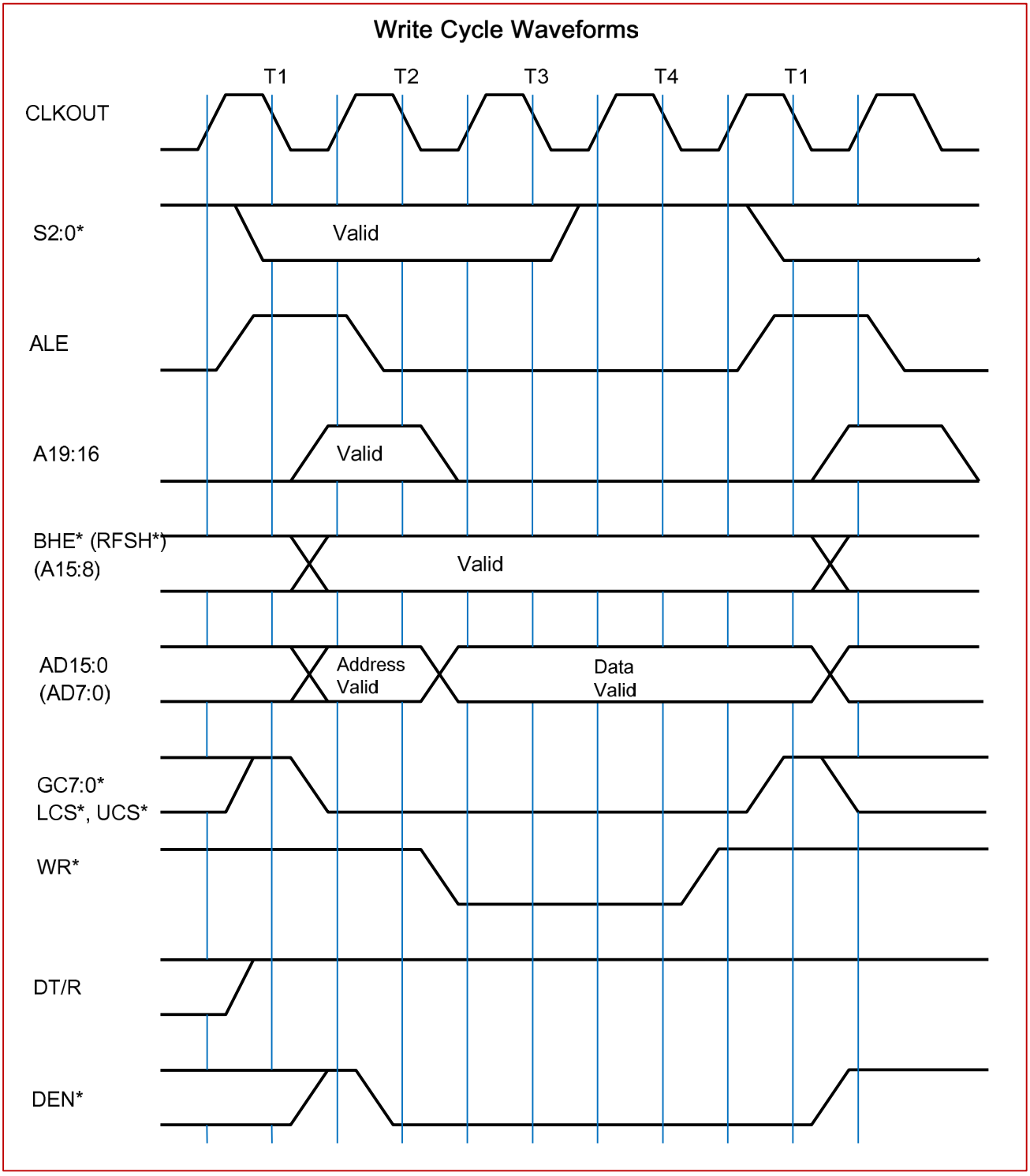
Input Setup and Hold Waveforms



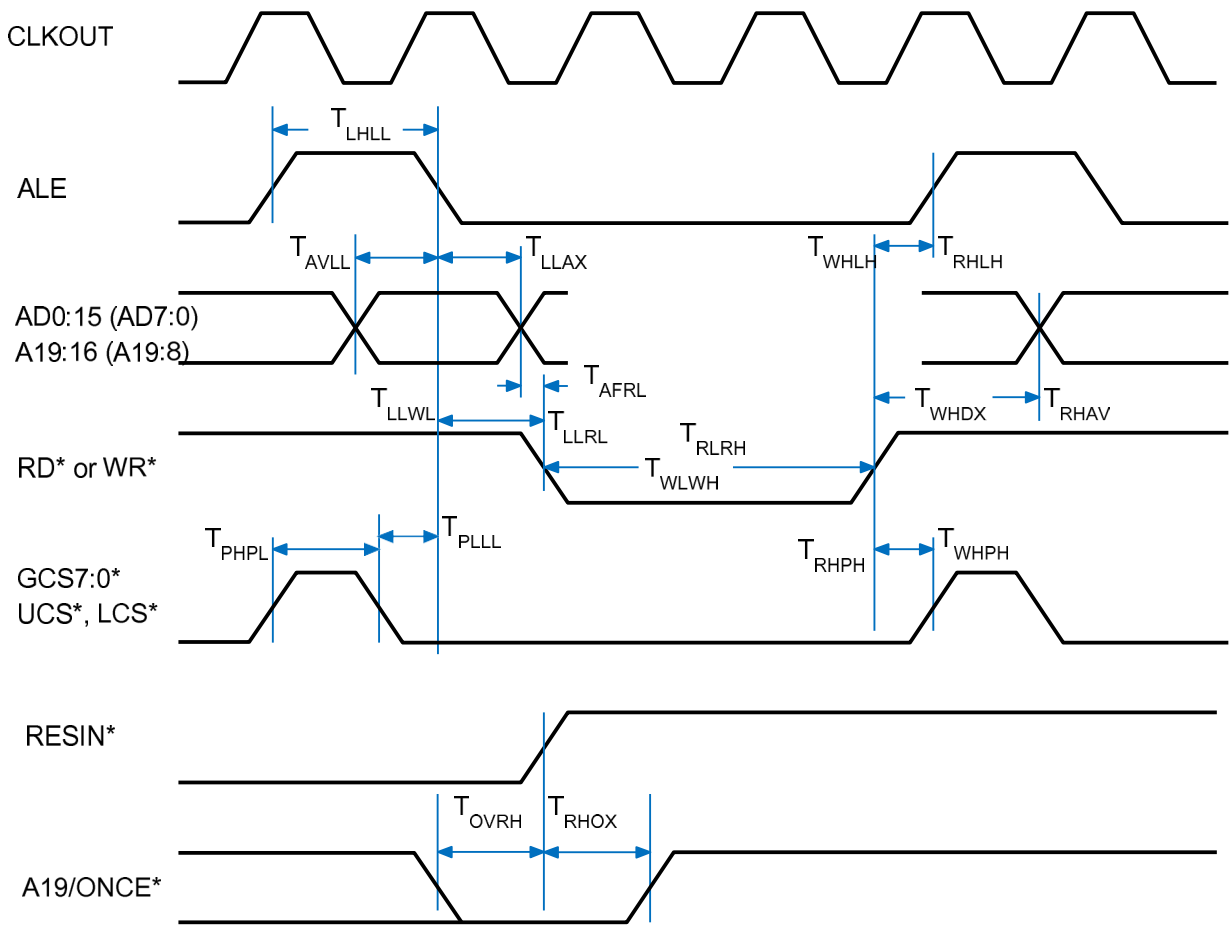
Read, Fetch, and Refresh Cycle Waveforms



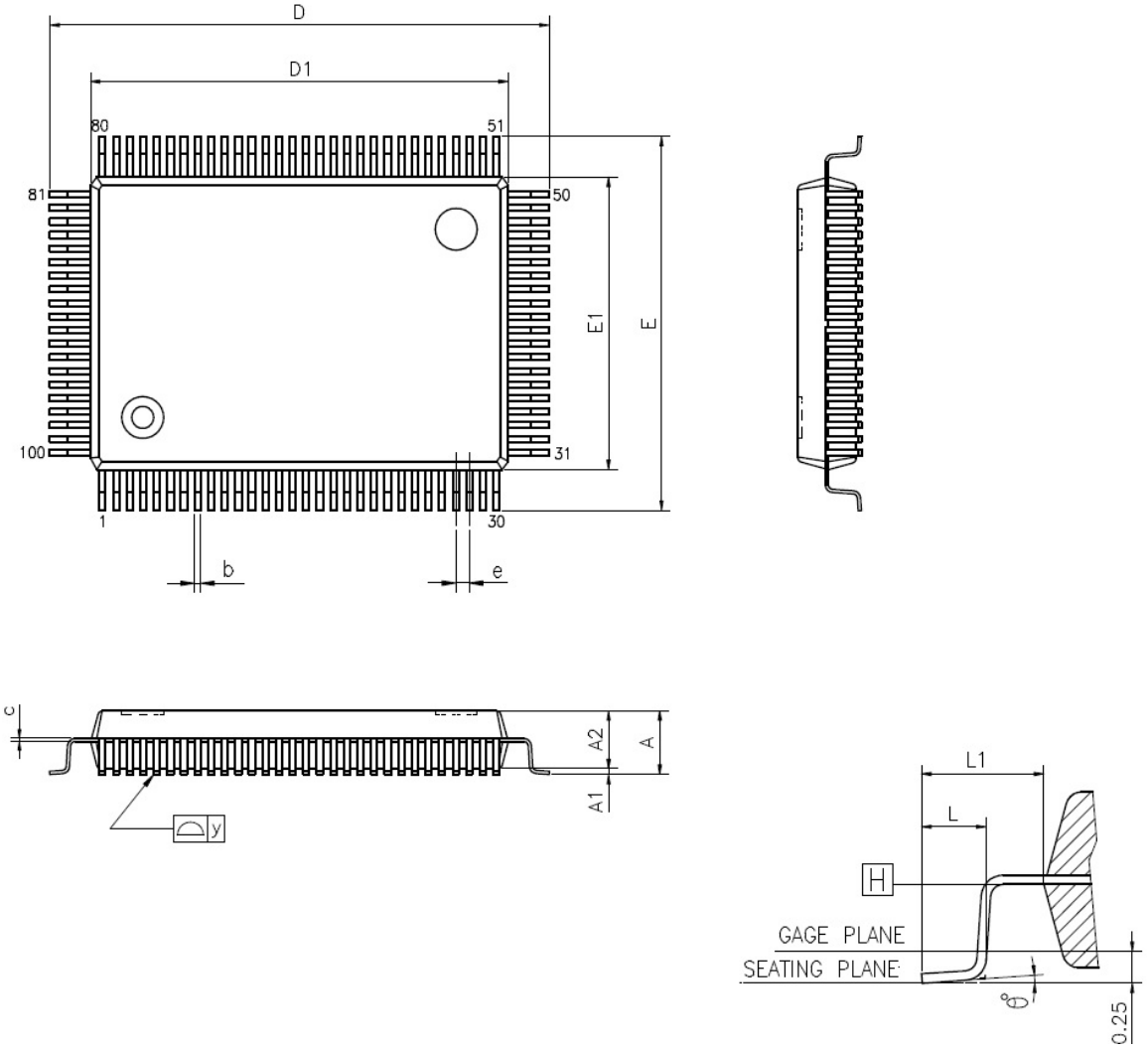
Write Cycle Waveforms



Relative Signal Waveforms



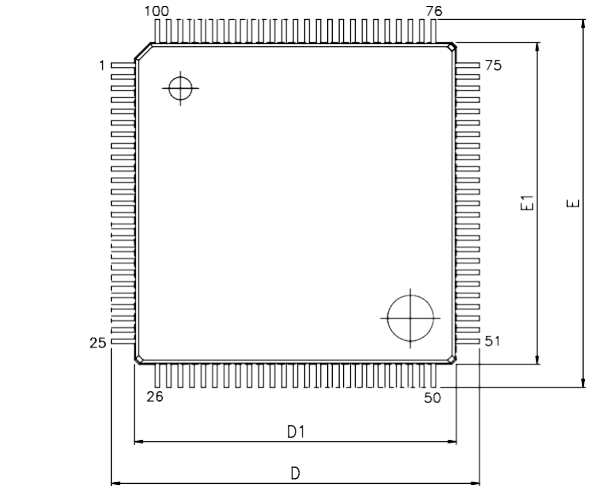
PQFP100 Package Mechanical Specifications

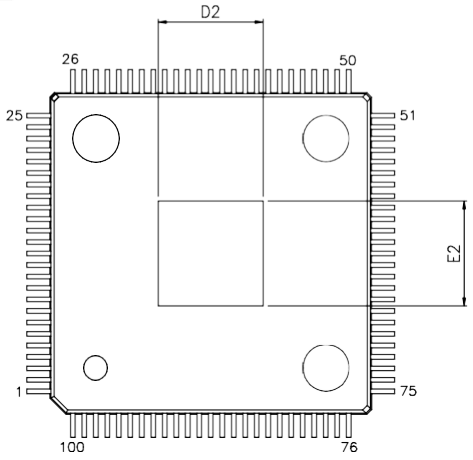


Dimension	Min	Nom	Max
A	-	-	-
A1	0.25	-	0.50
A2	2.50	-	2.90
b	0.20	0.30	2.40
c	0.10	0.15	0.20
D	23.80	23.90	24.00
D1	19.90	20.00	20.10
e	0.498	0.65	0.802
E	17.80	17.90	18.00
E1	13.90	14.00	14.10
L		1.00	
L1		1.95	
θ	0	-	7
y	-	-	0.10

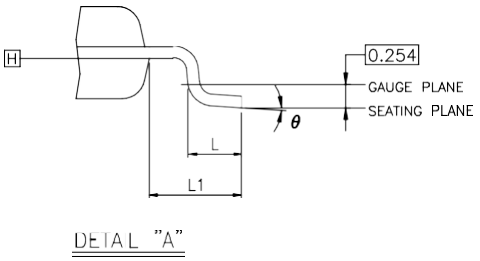
Dimensions in mm

Relative TQFP100 Package Mechanical Specifications





(THERMALLY ENHANCED VARIATIONS ONLY)



DETAIL "A"

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

Dimension	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	0.127	0.16
D		16.00 BSC	
D1		14.00 BSC	
E		16.00 BSC	
E1		14.00 BSC	
e		0.50 BSC	
L	0.45	0.58	0.75
L1		1.00 REF	
Θ	0°	3.5°	7°

THERMALLY ENHANCED DIMENSIONS (SHOWN IN MM)

PAD SIZE	E2		D2	
	MIN	MAX	MIN	MAX
180X18E	3.66	4.57	3.66	4.57
230X25E	4.97	5.84	4.97	5.84
256X25E	5.53	6.50	5.53	6.50

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Errata

1. The chip select signals are unnecessarily extended beyond the write strobes.

2. The READY pin on the TK80C186/EC does not extend the bus cycle. This is because the READY input is incorrectly connected to the Chip Select Unit. To extend a bus cycle for an external access, the work around is to program the appropriate chip select register (UCSST, LCSST, GCSxST). This solution has an upper limit of 15 Wait States.

Ordering Information

Reference Number	Ordering Number	Temperature	Package	Frequency	Replaces
TK80C186EC-25D	TK7737D	-40 to +85	Plastic 100 PQFP – RoHS	25 MHz	S80C186EC-25
TK80C186EC-25B	TK7737B	-40 to +85	Plastic 100 LQFP – RoHS	25 MHz	KU80C186EC-25
TK80C186EC-25K	TK7737K	-40 to +85	Adapter for 100 BQFP – RoHS	25 MHz	SB80C186EC-25
TK80C188EC-25D	TK7738D	-40 to +85	Plastic 100 PQFP – RoHS	25 MHz	S80C188EC-25
TK80C188EC-25B	TK7738B	-40 to +85	Plastic 100 LQFP – RoHS	25 MHz	KU80C188EC-25
TK80C188EC-25K	TK7738K	-40 to +85	Adapter for 100 BQFP – RoHS	25 MHz	SB80C188EC-25

Contact Information

The TK80C188 series may be ordered directly from Tekmos

Tekmos, Inc.
14121 Hwy 290 West
Building 15
Austin, TX 78737

512 342-9871 phone
Sales@Tekmos.Com
www.Tekmos.com

Revision History

Date	Revision	Description
1/15/14	1.0	Initial release
1/21/14	1.1	Include package mechanical data
2/11/14	1.2	Add note on solderability
3/28/18	1.3	Add LQFP & BQFP Package, update address and Logo
11/18/19	1.4	Updated Tekmos logo
7/9/20	1.5	changed LQFP to TQFP. Added TQFP Package Mechanical Data
05/14/2024	1.6	Added ordering numbers to Ordering Information Table