Errata

1. The ability to read the status of an external level sensitive interrupt is blocked by the mask bits. This can affect some polled interrupt applications.
2. The chip select signals are unnecessarily extended beyond the write strobes.
3. The chip select outputs are undefined after reset until the first memory cycle has been started. This could result in inadvertent chip selects being generated.
4. The READY pin on the TK80C186/EB does not extend the bus cycle. This is because the READY input is incorrectly connected to the Chip Select Unit. To extend a bus cycle for an external access, the work around is to program the appropriate chip select register (UCSST, LCSST, GCSxST). This solution has an upper limit of 15 Wait States.
5. The ADC AX, CX instruction fails to set the carry flag when the value of CX is FFFF. It works correctly for all other values of CX

Revision Table:

Revision	Description	Date
1.0	Initial Release	01/30/2024
2.0	Second Release	08/17/2026