TK68HC811E2 Microcontroller
512 Bytes RAM, 2048 bytes EEPROM

February 13th, 2024 V1.14 **Product Overview**

Features

- 175ºC Operation
- Enhanced screening for longer data retention.
- 68HC11 Central Processing Unit (CPU)
- Power Saving STOP and WAIT Modes
- 512 Bytes of On-Chip RAM, Data Retained During Standby
- 2048 Bytes Electrically Erasable Programmable ROM (EEPROM)
- Asynchronous Non-Return to Zero (NRZ) ` Communications Interface (SCI)
- Synchronous Serial Peripheral Interface (SPI)
- 8-Channel 8-Bit Analog-to-Digital (A/D) Converter
- 16-Bit Timer System
    - Three Input Capture (IC) Channels
    - Four Output Compare (OC) Channels
    - One Additional Channel, Selectable as Fourth IC or Fifth OC
- 8-Bit Pulse Accumulator
- Real-Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog System
- 38 General-Purpose Input / Output (I/O) Pins
    - 16 Bidirectional I/O Pins
    - 11 Input-Only Pins
    - 11 Output-Only Pins
- 48-Pin Ceramic Dual In-Line Package (DIP)
- Pin for pin replacement of the Freescale MC68HC811E2

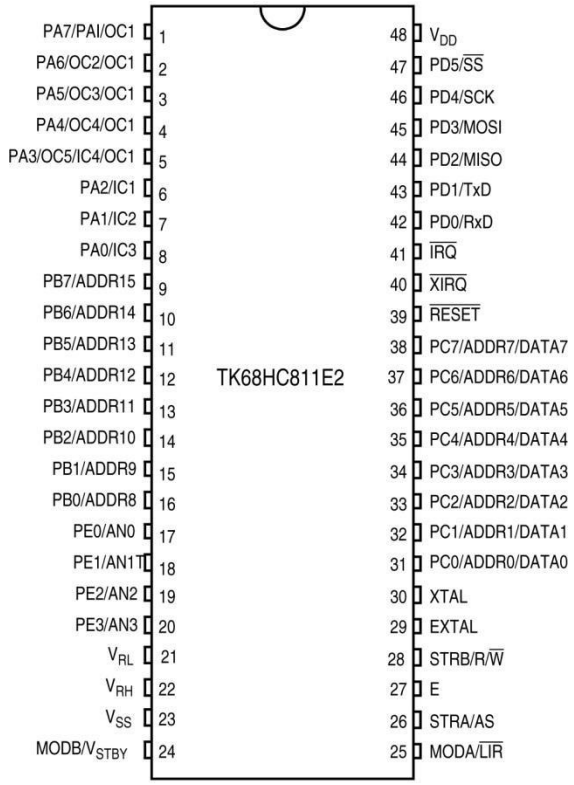
General Description

The TK68HC811E2 is a member of the TK68HC11E family of MCUs. The full set of specifications can be found in the datasheet TK68HC11E. The operation of the entire family is largely the same except for the various configurations of RAM, ROM, or EPROM.

The Tekmos TK68HC811E2 is available in a 175C version.

The TK68HC811E2 is a fully static design using high-density complementary metal-oxide semiconductor (HCMOS) fabrication process that allows it to operate at frequencies from 2 MHz to dc, with very low power consumption.

The device is available in the 48 pin Ceramic DIP, the 52-pin PLCC, and the 52 pin PQFP packages.



Pin Assignments for 48-Pin DIP

Pinout

PLCC	CDIP	PQFP	Signal		PLCC	CDIP	PQFP	Signal
1	23	46	VSS		52	22	45	VRH
2	24	47	MODB		51	21	44	VRL
3	25	48	MODA		50		43	PE7
4	26	49	STRA		49	20	42	PE3
5	27	50	E		48		41	PE6
6	28	51	STRB		47	19	40	PE2
7	29	52	EXTAL		46		39	PE5
8	30	1	XTAL		45	18	38	PE1
9	31	2	PC0		44		37	PE4
10	32	3	PC1		43	17	36	PE0
11	33	4	PC2		42	16	35	PB0
12	34	5	PC3		41	15	34	PB1
13	35	6	PC4		40	14	33	PB2
14	36	7	PC5		39	13	32	PB3
15	37	8	PC6		38	12	31	PB4
16	38	9	PC7		37	11	30	PB5
17	39	10	/RESET		36	10	29	PB6
18	40	11	/XIRQ		35	9	28	PB7
19	41	12	/IRQ		34	8	27	PA0
20	42	13	PD0		33	7	26	PA1
21	43	14	PD1		32	6	25	PA2
22	44	15	PD2		31	5	24	PA3
23	45	16	PD3		30	4	23	PA4
24	46	17	PD4		29	3	22	PA5
25	47	18	PD5		28	2	21	PA6
26	48	19	VDD		27	1	20	PA7

Electrical Characteristics

5.1 General Requirements - All static and dynamic electrical characteristics specified.

5.2 – Static Characteristics

5.2.1 DC Electrical Characteristics

Characteristics[1]	Symbol	Min	Max	Unit
Output voltage[2] I_{Load} = ±±10.0 µA All outputs except XTAL All outputs except XTAL, $\overline{\text{RESET}}$, and MODA	V_{OL}, V_{OH}	— V_{DD} –0.1	0.1 —	V
Output high voltage[2] I_{Load} = –0.8 mA, V_{DD} = 4.5 V All outputs except XTAL, $\overline{\text{RESET}}$, and MODA	V_{OH}	V_{DD} –0.8	—	V
Output low voltage I_{Load} = 1.6 mA All outputs except XTAL	V_{OL}	—	0.4	V
Input high voltage All inputs except $\overline{\text{RESET}}$ $\overline{\text{RESET}}$	V_{IH}	0.7 × V_{DD} 0.8 × V_{DD}	V_{DD} + 0.3 V_{DD} + 0.3	V
Input low voltage, all inputs	V_{IL}	V_{SS} –0.3	0.2 × V_{DD}	V
I/O ports, 3-state leakage V_{In} = V_{IH} or V_{IL} PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$	I_{OZ}	—	±10	µA
Input leakage current V_{In} = V_{DD} or V_{SS} PA[2:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$ MODB/V_{STBY} ($\overline{\text{XIRQ}}$ on EPROM-based devices)	I_{In}	— —	±1 ±10	µA
RAM standby voltage, power down	V_{SB}	4.0	V_{DD}	V
RAM standby current, power down	I_{SB}	—	10	µA
Input capacitance PA[2:0], PE[7:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$, EXTAL PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$	C_{In}	— —	8 12	pF
Output load capacitance All outputs except PD[4:1] PD[4:1]	C_L	— —	90 100	pF

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted
2. V_{OH} specification for $\overline{\text{RESET}}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wired-OR mode.

5.2.2 Supply Currents and Power Dissipation

Characteristics[1]	Symbol	Min	Max	Unit
Run maximum total supply current[2]				
Single-chip mode2 MHz	I_{DD}	—	15	mA
3 MHz		—	27	
Expanded multiplexed mode2 MHz		—	27	
3 MHz		—	35	
Wait maximum total supply current[2] (all peripheral functions shut down)				
Single-chip mode2 MHz	W_{IDD}	—	6	mA
3 MHz		—	15	
Expanded multiplexed mode2 MHz		—	10	
3 MHz		—	20	
Stop maximum total supply current[2]				
Single-chip mode, no clocks–40°C to +85°C	S_{IDD}	—	25	µA
> +85°C to +105°C		—	50	
> +105°C to +125°C		—	100	
Maximum power dissipation				
Single-chip mode2 MHz	P_D	—	85	mW
3 MHz		—	150	
Expanded multiplexed mode2 MHz		—	150	
3 MHz		—	195	

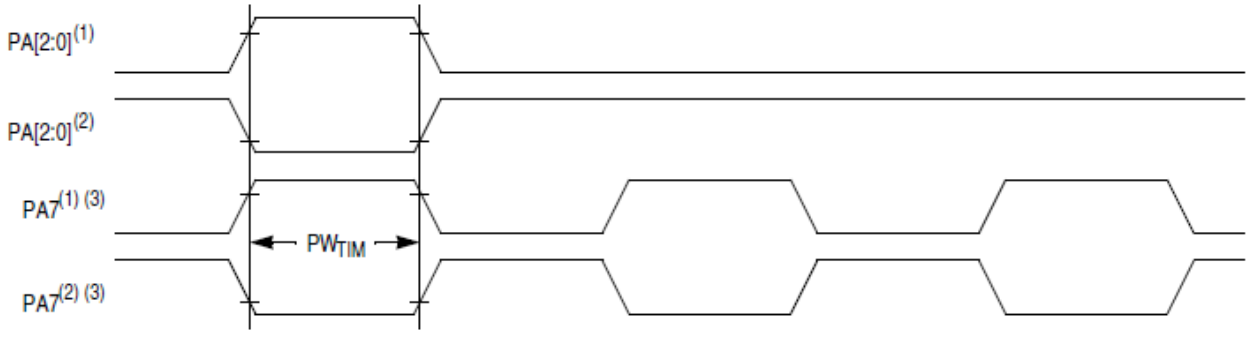
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted
2. EXTAL is driven with a square wave, and
   t_{CYC}= 500 ns for 2 MHz rating
   t_{CYC}= 333 ns for 3 MHz rating
   $V_{IL} \le 0.2$ V
   $V_{IH} \ge V_{DD} - 0.2$ V
   no dc loads

5.3 Dynamic (Switching) characteristics
5.3.1 Control Timing

Characteristic[1] [2]	Symbol	1.0 MHz		2.0 MHz		Unit
		Min	Max	Min	Max	
Frequency of operation	f_o	dc	1.0	dc	2.0	MHz
E-clock period	t_{CYC}	1000	—	500	—	ns
Crystal frequency	f_{XTAL}	—	4.0	—	8.0	MHz
External oscillator frequency	4 f_o	dc	4.0	dc	8.0	MHz
Processor control setup time t_{PCSU} = 1/4 t_{CYC}+ 50 ns	t_{PCSU}	300	—	175	—	ns
Reset input pulse width To guarantee external reset vector Minimum input time (can be pre-empted by internal reset)	PW_{RSTL}	8 1	— —	8 1	— —	t_{CYC}
Mode programming setup time	t_{MPS}	2	—	2	—	t_{CYC}
Mode programming hold time	t_{MPH}	10	—	10	—	ns
Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode PW_{IRQ} = t_{CYC} + 20 ns	PW_{IRQ}	1020	—	520	—	ns
Wait recovery startup time	t_{WRS}	—	4	—	4	t_{CYC}
Timer pulse width input capture pulse accumulator input PW_{TIM} = t_{CYC} + 20 ns	PW_{TIM}	1020	—	520	—	ns

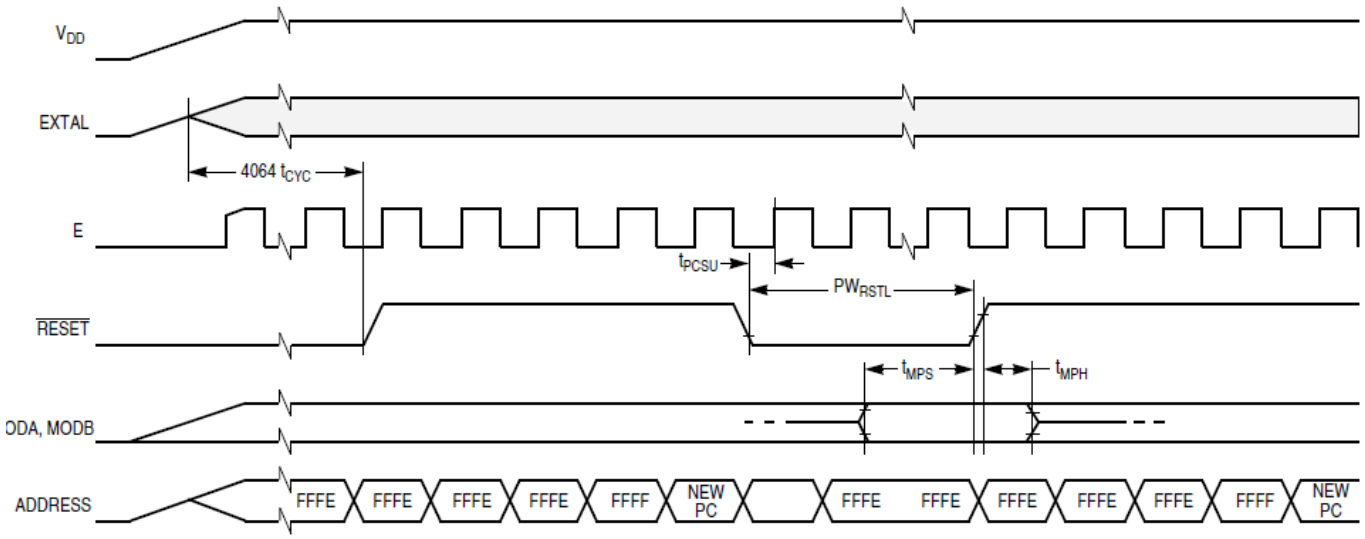
1. V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, all timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted
2. $\overline{RESET}$ is recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt.

Timer Inputs

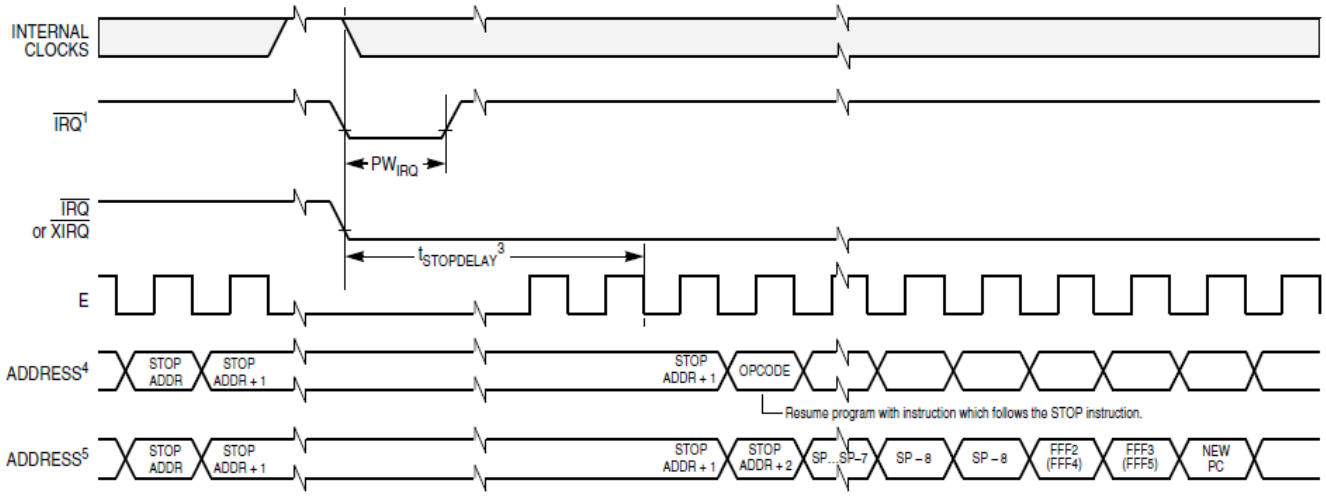


Notes:
1. Rising edge sensitive input
2. Falling edge sensitive input
3. Maximum pulse accumulator clocking rate is E-clock frequency divided by 2.

POR External Reset Timing Diagram

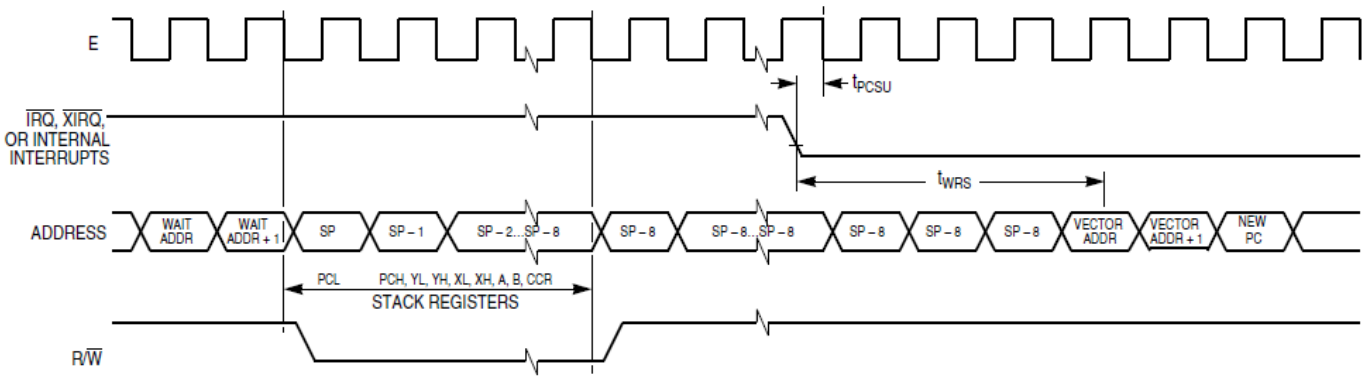


STOP Recovery Timing Diagram



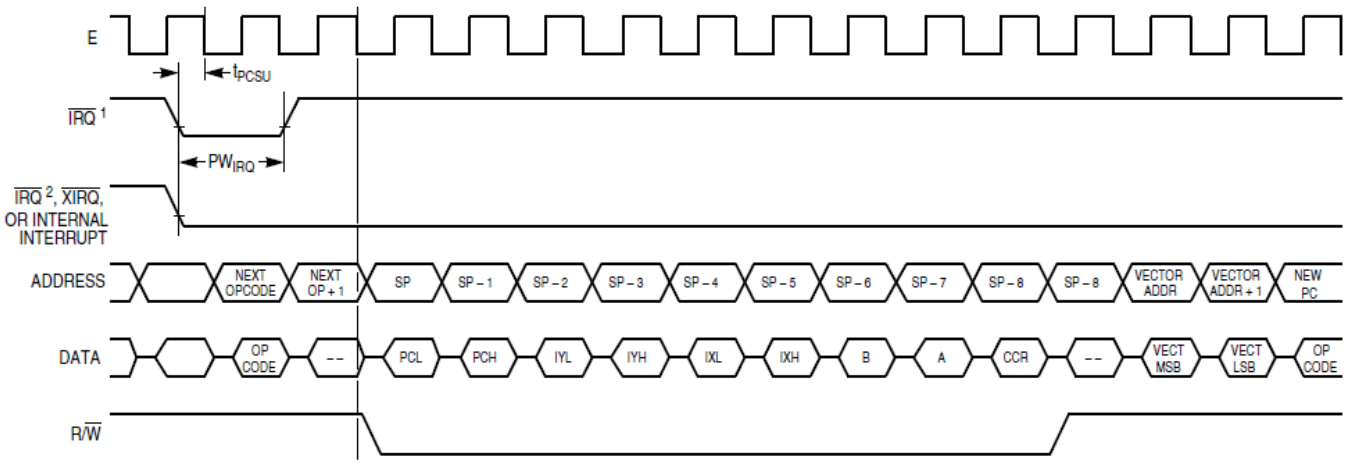
Notes:
1. Edge Sensitive $\overline{IRQ}$ pin (IRQE bit = 1)
2. Level sensitive $\overline{IRQ}$ pin (IRQE bit = 0)
3. $t_{STOPDELAY}$ = 4064 t_{CYC} if DLY bit = 1 or 4 t_{CYC} if DLY = 0.
4. $\overline{XIRQ}$ with X bit in CCR = 1.
5. $\overline{IRQ}$ or ($\overline{XIRQ}$ with X bit in CCR = 0).

WAIT Recovery from Interrupt Timing Diagram



Note: RESET also causes recovery from WAIT.

Interrupt Timing Diagram



Notes:
1. Edge sensitive IRQ pin (IRQE bit = 1)
2. Level sensitive IRQ pin (IRQE bit = 0)

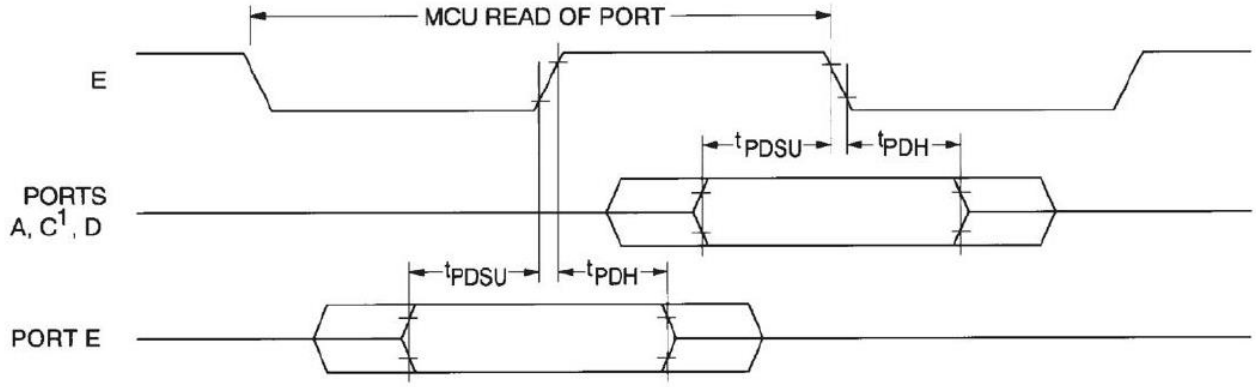
5.3.2 Peripheral Port Timing

10.11 Peripheral Port Timing

Characteristic[1] [2]	Symbol	1.0 MHz		2.0 MHz		Unit
		Min	Max	Min	Max	
Frequency of operation E-clock frequency	f_o	dc	1.0	dc	2.0	MHz
E-clock period	t_{CYC}	1000	—	500	—	ns
Peripheral data setup time MCU read of ports A, C, D, and E	t_{PDSU}	100	—	100	—	ns
Peripheral data hold time MCU read of ports A, C, D, and E	t_{PDH}	50	—	50	—	ns
Delay time, peripheral data write t_{PWD} = 1/4 t_{CYC}+ 100 ns MCU writes to port A MCU writes to ports B, C, and D	t_{PWD}	 — —	 200 350	 — —	 200 225	ns
Port C input data setup time	t_{IS}	60	—	60	—	ns
Port C input data hold time	t_{IH}	100	—	100	—	ns
Delay time, E fall to STRB t_{DEB} = 1/4 t_{CYC}+ 100 ns	t_{DEB}	—	350	—	225	ns
Setup time, STRA asserted to E fall[3]	t_{AES}	0	—	0	—	ns
Delay time, STRA asserted to port C data output valid	t_{PCD}	—	100	—	100	ns
Hold time, STRA negated to port C data	t_{PCH}	10	—	10	—	ns
3-state hold time	t_{PCZ}	—	150	—	150	ns

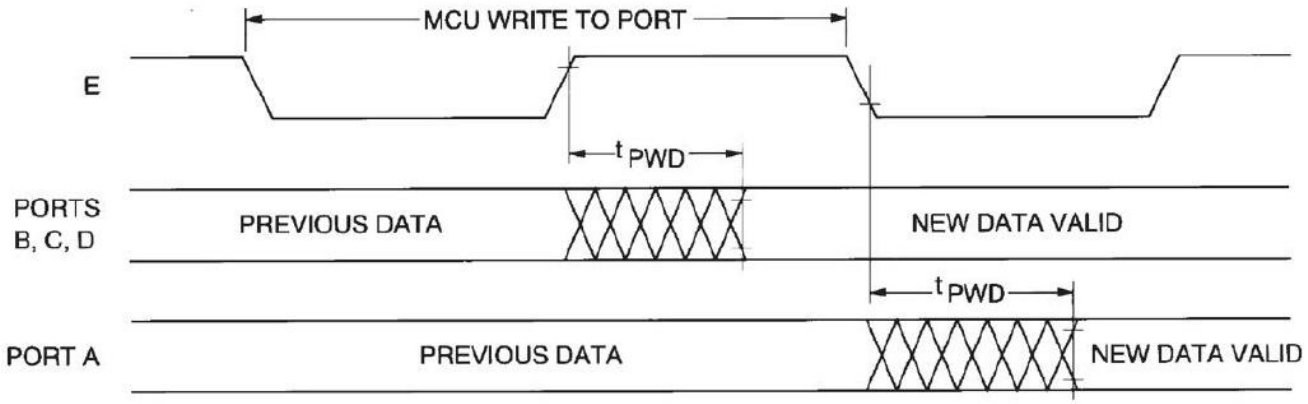
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, all timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted
2. Ports C and D timing is valid for active drive. (CWOM and DWOM bits are not set in PIOC and SPCR registers, respectively.)
3. If this setup time is met, STRB acknowledges in the next cycle. If it is not met, the response may be delayed one more cycle.

Port Read Timing Diagram

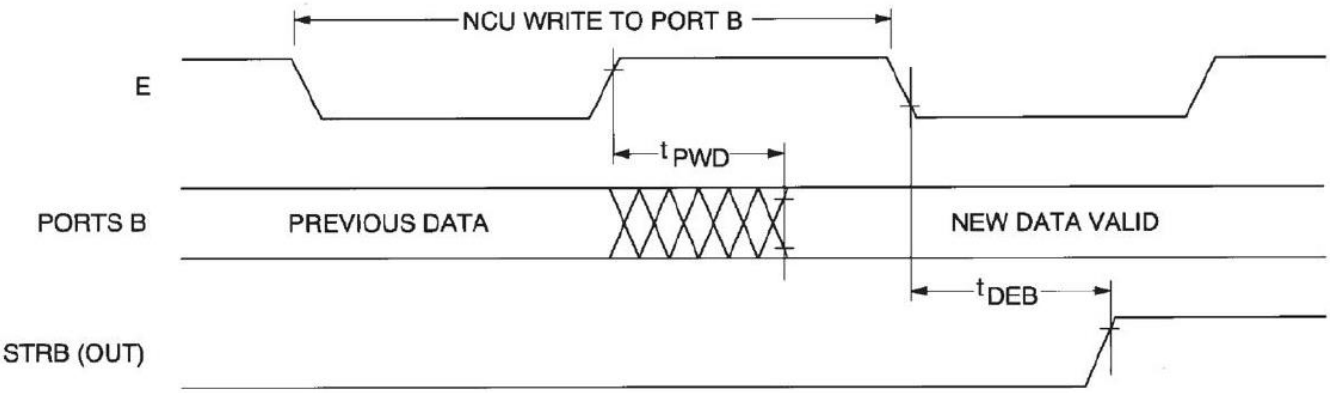


Note : For non-latched operation of Port C.

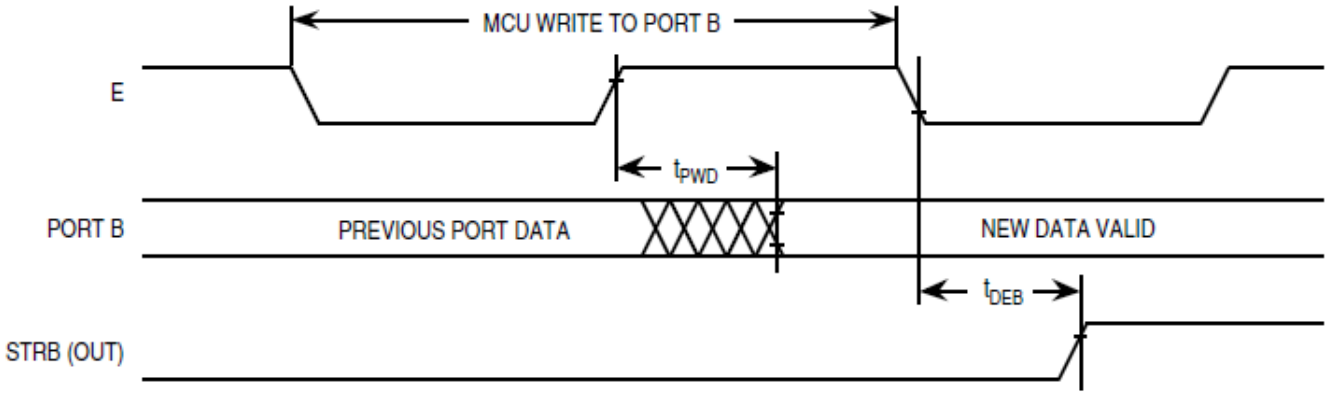
Port Write Timing Diagram



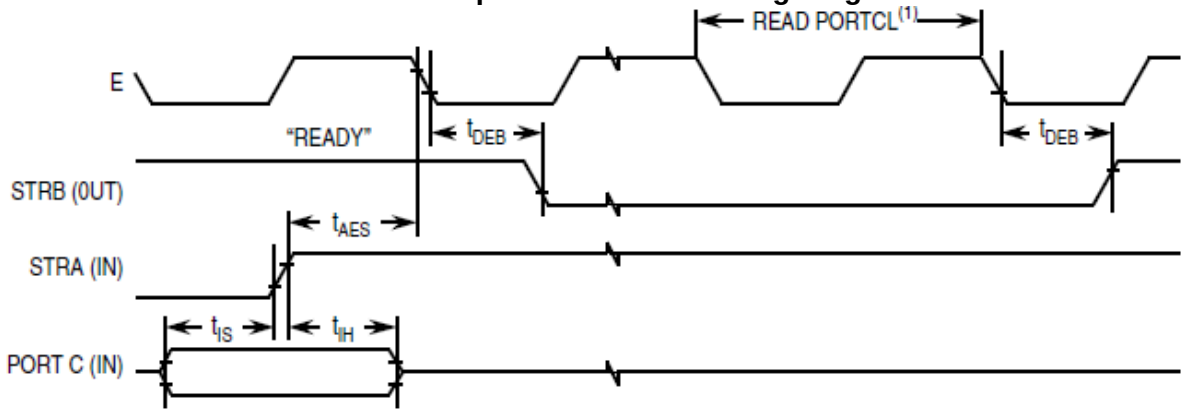
Simple Input Strobe Timing Diagram



Simple Output Strobe Timing Diagram

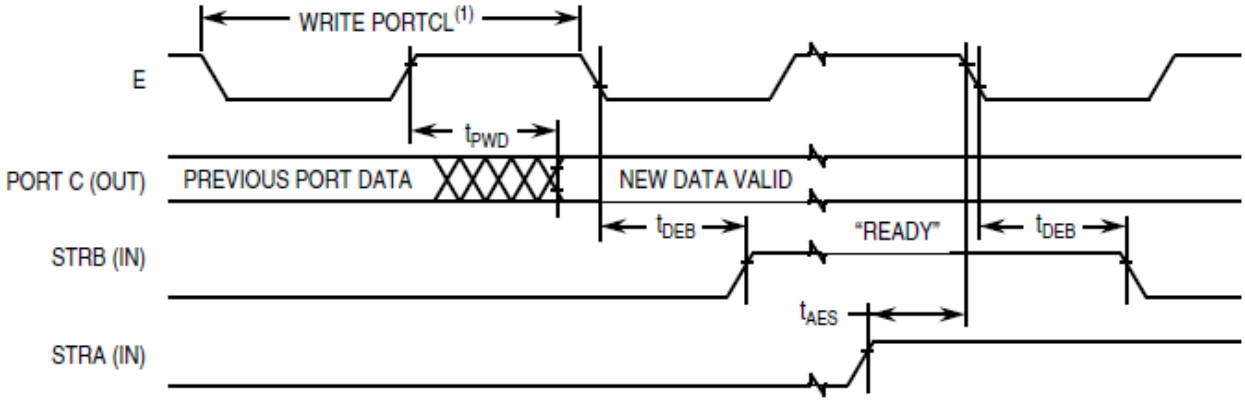


Port C Input Handshake Timing Diagram



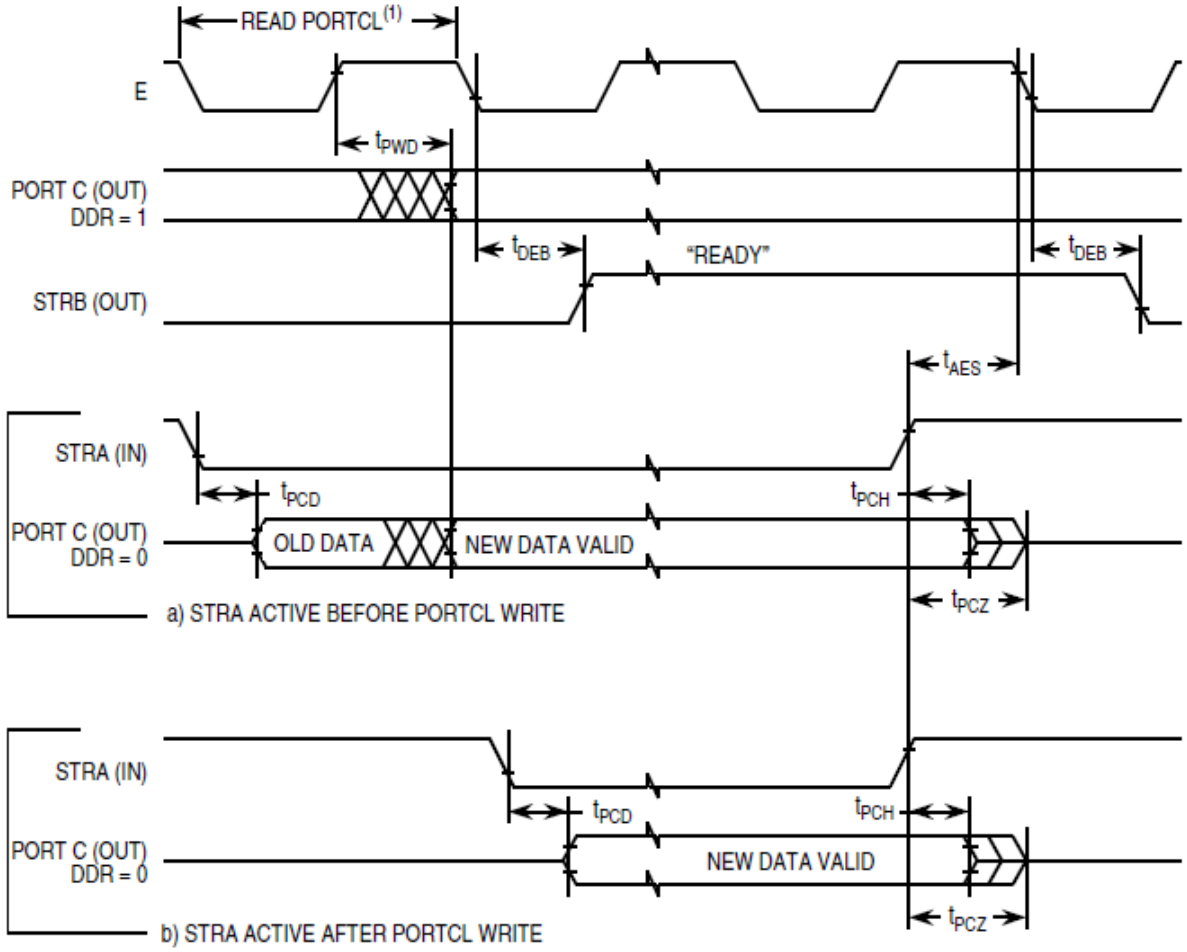
Notes:
1. After reading PIOC with STAF set
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

Port C Output Handshake Timing Diagram



Notes:
1. After reading PIOC with STAF set
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

State Variation of Output Handshake Timing Diagram
(STRA Enables Output Buffer)



Notes:
1. After reading PIOC with STAF set
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

5.4 Analog-to-Digital Converter Characteristics

Characteristic[1]	Parameter[2]	Min	Absolute	2.0 MHz Max	Unit
Resolution	Number of bits resolved by A/D converter	—	8	—	Bits
Non-linearity	Maximum deviation from the ideal A/D transfer characteristics	—	—	±1/2	LSB
Zero error	Difference between the output of an ideal and an actual for 0 input voltage	—	—	±1/2	LSB
Full scale error	Difference between the output of an ideal and an actual A/D for full-scale input voltage	—	—	±1/2	LSB
Total unadjusted error	Maximum sum of non-linearity, zero error, and full-scale error	—	—	±1/2	LSB
Quantization error	Uncertainty because of converter resolution	—	—	±1/2	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	—	—	±1	LSB
Conversion range	Analog input voltage range	V_{RL}	—	V_{RH}	V
V_{RH}	Maximum analog reference voltage[3]	V_{RL}	—	V_{DD} +0.1	V
V_{RL}	Minimum analog reference voltage[2]	V_{SS} –0.1	—	V_{RH}	V
ΔV_R	Minimum difference between V_{RH} and V_{RL}[2]	3	—	—	V
Conversion time	Total time to perform a single A/D conversion: E clock Internal RC oscillator	 — —	 32 —	 — t_{CYC}+32	 t_{CY} µs
Monotonicity	Conversion result never decreases with an increase in input voltage; has no missing codes	—	Guaranteed	—	—
Zero input reading	Conversion result when $V_{In} = V_{RL}$	00	—	—	Hex
Full scale reading	Conversion result when $V_{In} = V_{RH}$	—	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling time: E clock Internal RC oscillator	 — —	 12 —	 — 12	 t_{CY} µs
Sample/hold capacitance	Input capacitance during sample PE[7:0]	—	20 typical	—	pF
Input leakage	Input leakage on A/D pins PE[7:0] V_{RL}, V_{RH}	 — —	 — —	 400 1.0	 nA µA

1. V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, 750 kHz ≤ E ≤ 3.0 MHz, unless otherwise noted
2. Source impedances greater than 10 kΩ affect accuracy adversely because of input leakage.
3. Performance verified down to 2.5 V ΔV_R, but accuracy is tested and guaranteed at ΔV_R = 5 V ±10%.

5.5 Expansion Bus Timing Characteristics

Num	Characteristic[1]	Symbol	1.0 MHz		2.0 MHz		Unit
			Min	Max	Min	Max	
	Frequency of operation (E-clock frequency)	f_o	dc	1.0	dc	2.0	MHz
1	Cycle time	t_{CYC}	1000	—	500	—	ns
2	Pulse width, E low[2], PW_{EL} = 1/2 t_{CYC}–23 ns	PW_{EL}	477	—	227	—	ns
3	Pulse width, E high[2], PW_{EH} = 1/2 t_{CYC}–28 ns	PW_{EH}	472	—	222	—	ns
4a	E and AS rise time	t_r	—	20	—	20	ns
4b	E and AS fall time	t_f	—	20	—	20	ns
9	Address hold time[2] [3]a, t_{AH} = 1/8 t_{CYC}–29.5 ns	t_{AH}	95.5	—	33	—	ns
12	Non-multiplexed address valid time to E rise $t_{AV} = PW_{EL} - (t_{ASD} + 80\ ns)$[2] [3]a	t_{AV}	281.5	—	94	—	ns
17	Read data setup time	t_{DSR}	30	—	30	—	ns
18	Read data hold time, max = t_{MAD}	t_{DHR}	0	145.5	0	83	ns
19	Write data delay time, t_{DDW} = 1/8 t_{CYC}+ 65.5 ns[2] [3]a	t_{DDW}	—	190.5	—	128	ns
21	Write data hold time, t_{DHW} = 1/8 t_{CYC}–29.5 ns[2] [3]a	t_{DHW}	95.5	—	33	—	ns
22	Multiplexed address valid time to E rise $t_{AVM} = PW_{EL} - (t_{ASD} + 90\ ns)$[2] [3]a	t_{AVM}	271.5	—	84	—	ns
24	Multiplexed address valid time to AS fall $t_{ASL} = PW_{ASH} - 70\ ns$[2]	t_{ASL}	151	—	26	—	ns
25	Multiplexed address hold time t_{AHL} = 1/8 t_{CYC}–29.5 ns[2] [3]b	t_{AHL}	95.5	—	33	—	ns
26	Delay time, E to AS rise, t_{ASD} = 1/8 t_{CYC}–9.5 ns[2] [3]a	t_{ASD}	115.5	—	53	—	ns
27	Pulse width, AS high, PW_{ASH} = 1/4 t_{CYC}–29 ns[2]	PW_{ASH}	221	—	96	—	ns
28	Delay time, AS to E rise, t_{ASED} = 1/8 t_{CYC}–9.5 ns[2] [3]b	t_{ASED}	115.5	—	53	—	ns
29	MPU address access time[3]a $t_{ACCA} = t_{CYC} - (PW_{EL} - t_{AVM}) - t_{DSR} - t_f$	t_{ACCA}	744.5	—	307	—	ns
35	MPU access time, $t_{ACCE} = PW_{EH} - t_{DSR}$	t_{ACCE}	—	442	—	192	ns
36	Multiplexed address delay (Previous cycle MPU read) $t_{MAD} = t_{ASD} + 30\ ns$[2] [3]a	t_{MAD}	145.5	—	83	—	ns

1. V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, all timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted
2. Formula only for dc to 2 MHz
3. Input clocks with duty cycles other than 50% affect bus performance. Timing parameters affected by input clock duty cycle are identified by (a) and (b). To recalculate the approximate bus timing values, substitute the following expressions in place of 1/8 t_{CYC} in the above formulas, where applicable:
   (a) (1–dc) × 1/4 t_{CYC}
   (b) dc × 1/4 t_{CYC}

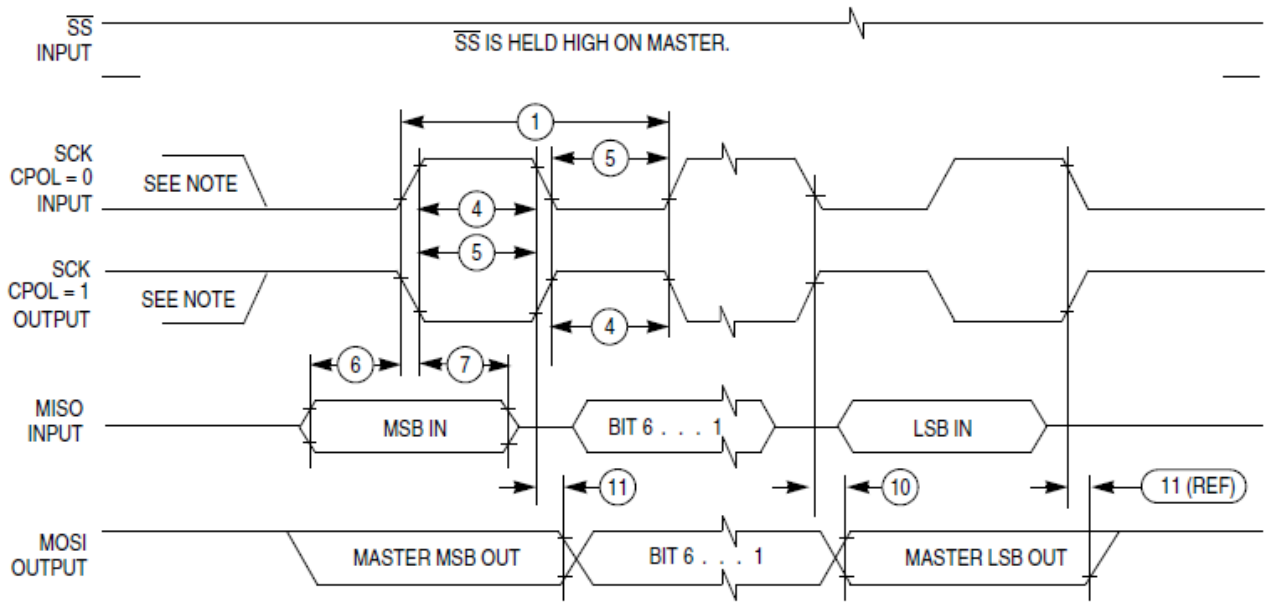
Where:
dc is the decimal value of duty cycle percentage (high time)

5.6 Serial Peripheral Interface Timing Characteristics

Num	Characteristic[1]	Symbol	Min	Max	Unit
	Frequency of operation E clock	f_o	dc	2.0	MHz
	E-clock period	t_{CYC}	333	—	ns
	Operating frequency Master Slave	 $f_{op(m)}$ $f_{op(s)}$	 $f_o/32$ dc	 $f_o/2$ f_o	MHz
1	Cycle time Master Slave	 $t_{CYC(m)}$ $t_{CYC(s)}$	 2 1	 32 —	t_{CYC}
2	Enable lead time[2] Slave	$t_{lead(s)}$	1	—	t_{CYC}
3	Enable lag time[2] Slave	$t_{lag(s)}$	1	—	t_{CYC}
4	Clock (SCK) high time Master Slave	 $t_{w(SCKH)m}$ $t_{w(SCKH)s}$	 $t_{CYC}-25$ 1/2 $t_{CYC}-25$	 16 t_{CYC} —	ns
5	Clock (SCK) low time Master Slave	 $t_{w(SCKL)m}$ $t_{w(SCKL)s}$	 $t_{CYC}-25$ 1/2 $t_{CYC}-25$	 16 t_{CYC} —	ns
6	Data setup time (inputs) Master Slave	 $t_{su(m)}$ $t_{su(s)}$	 30 30	 — —	ns
7	Data hold time (inputs) Master Slave	 $t_{h(m)}$ $t_{h(s)}$	 30 30	 — —	ns
8	Slave access time CPHA = 0 CPHA = 1	t_a	 0 0	 40 40	ns
9	Disable time (hold time to high-impedance state) Slave	t_{dis}	—	50	ns
10	Data valid[3] (after enable edge)	t_v	—	50	ns
11	Data hold time (outputs) (after enable edge)	t_{ho}	0	—	ns

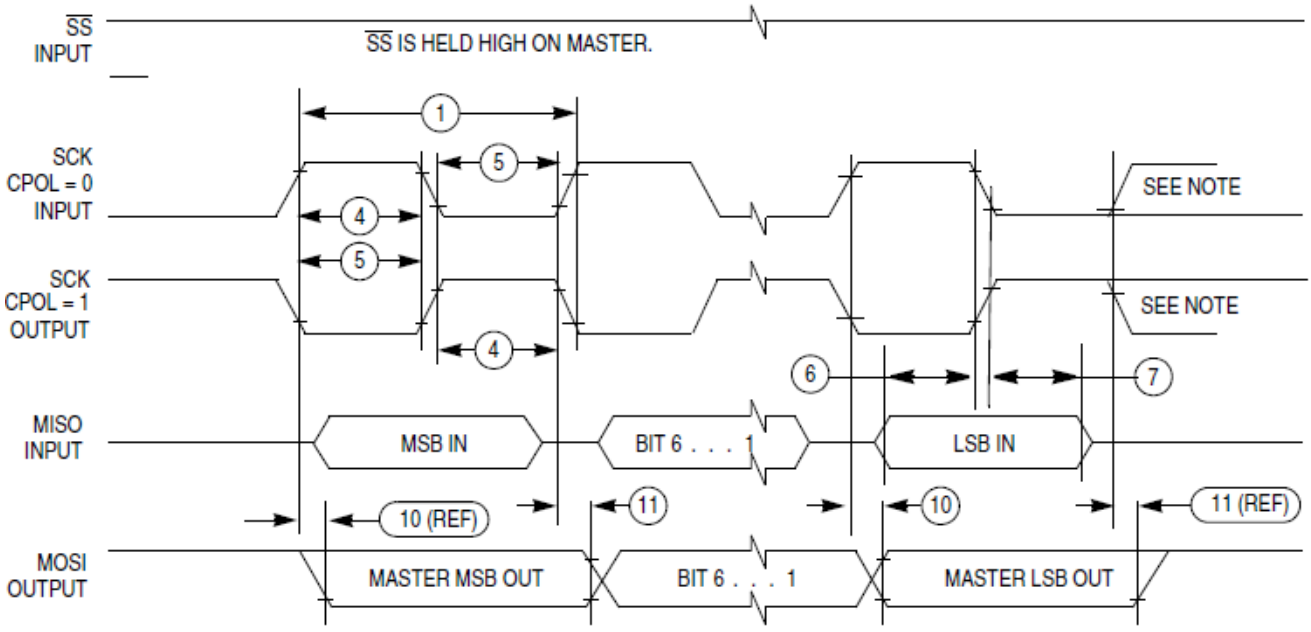
1. V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, all timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted
2. Time to data active from high-impedance state
3. Assumes 200 pF load on SCK, MOSI, and MISO pins

SPI Master Timing (CPHA = 0)



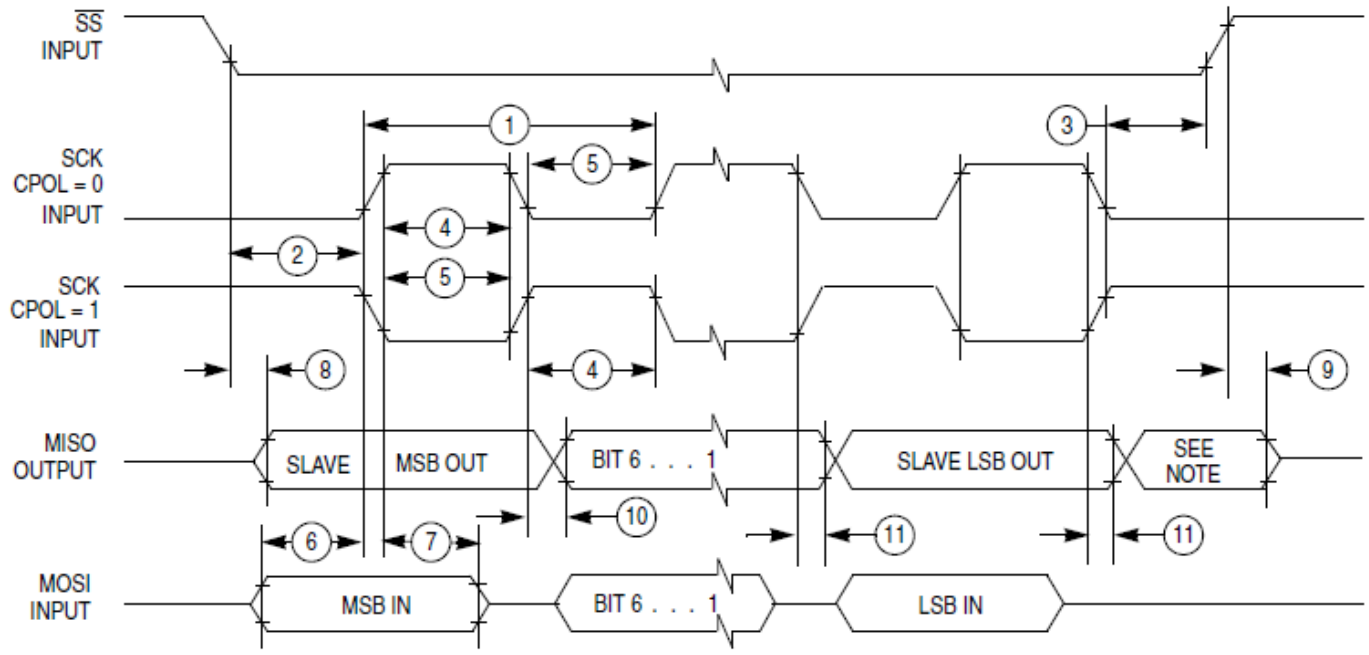
Note: This first clock edge is generated internally but is not seen at the SCK pin.

SPI Master Timing (CPHA = 1)



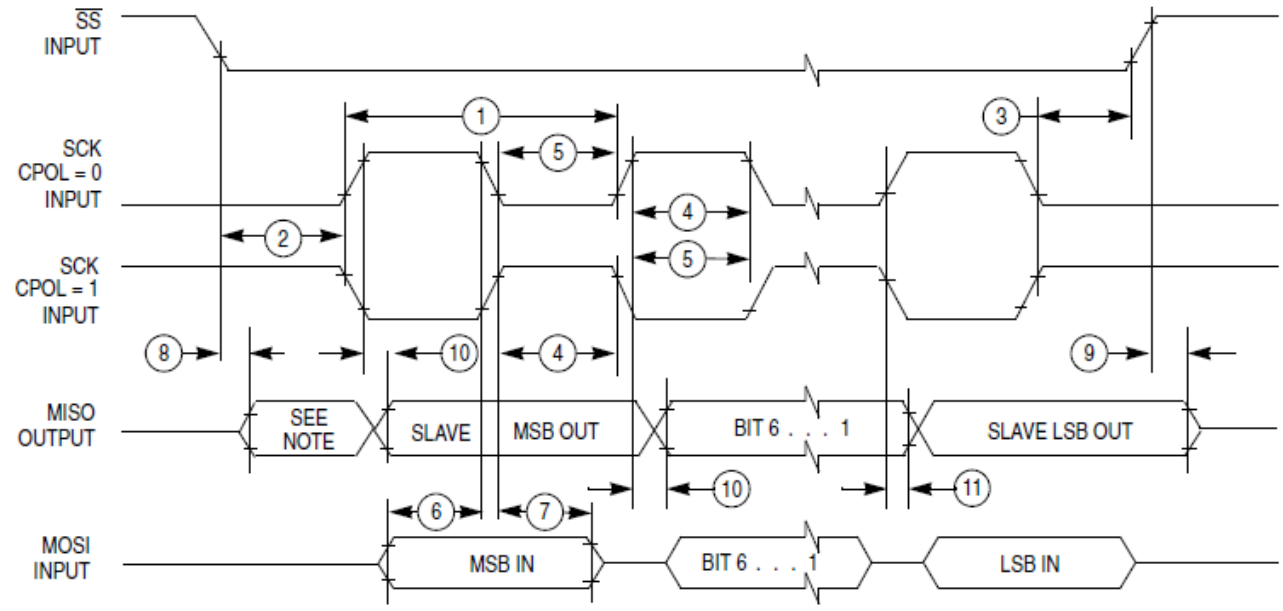
Note: This first clock edge is generated internally but is not seen at the SCK pin.

SPI Slave Timing (CPHA = 0)



Note: Not defined but normally MSB of character just received

SPI Slave Timing (CPHA = 1)



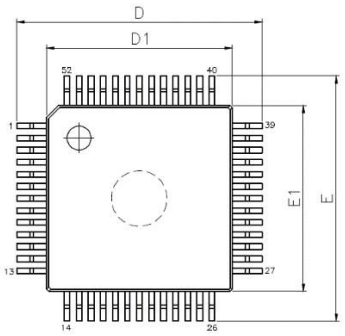
Note: Not defined but normally LSB of character previously transmitted

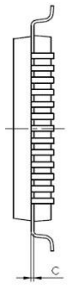
5.7 EEPROM Characteristics

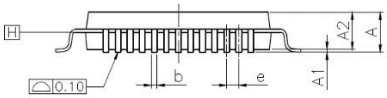
Characteristic[1]	Temperature Range			Unit
	–40 to 85°C	–40 to 125°C	–55 to 175°C	
Programming time	10	20	20	ms
Erase time Byte, row, and bulk	10	10	10	ms
Write/erase endurance	10,000	10,000	5,000	Cycles
Data retention	10	10	10	Years

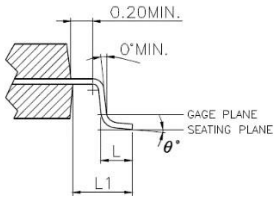
1. V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Package Outlines
PQFP 52Pin-









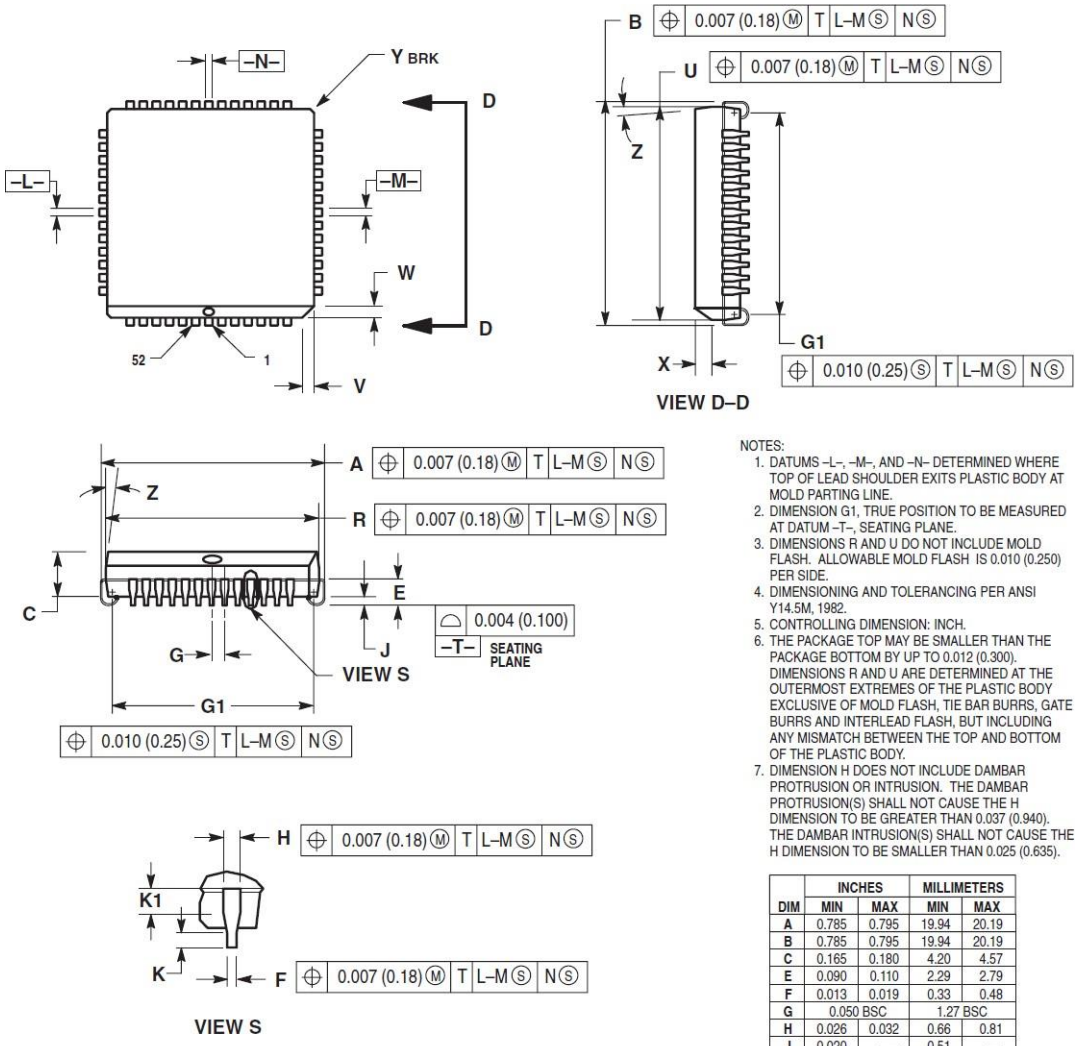
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	2.70
A1	0.25	–	0.50
A2	1.80	2.00	2.20
b	0.22	–	0.40
D	13.00	13.20	13.40
D1	9.90	10.00	10.10
E	13.00	13.20	13.40
E1	9.90	10.00	10.10
e	0.65 BASIC		
c	0.11	–	0.23
L	0.73	0.88	1.03
L1	1.60 REF.		
θ°	0	–	7

UNIT : MM

NOTES:

1. JEDEC OUTLINE : MO-108 AC-1
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H .
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

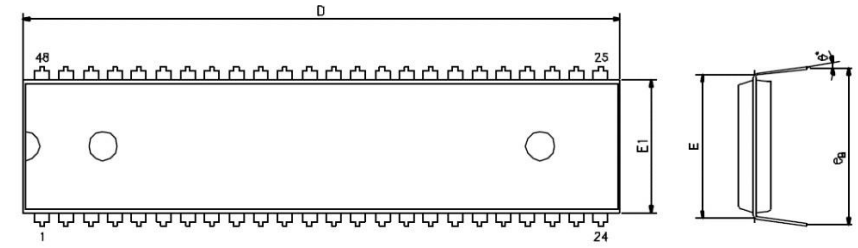
PLCC 52Pin-



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

Ceramic DIP 48Pin-



SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.220
A1	0.015	–	–
A2	0.150	0.155	0.160
D	2.400	2.450	2.550
E		0.600 BSC	
E1	0.540	0.545	0.550
L	0.115	0.130	0.150
e_B	0.630	0.650	0.670
θ°	0	7	15

UNIT : INCH

NOTE:
1.JEDEC OUTLINE : MS-011 AD

Ordering Information

All devices use the 7740 die revision.

Temperature	Frequency	Reference Number	Ordering Number	Package	Lead Finish
-40ºC to +125ºC	2 MHz	TK68HC811E2MC2	TK7740E	48 CDIP	RoHS
-55ºC to +175ºC	2 MHz	TK68HC811E2XSE2	TK7740	48 CDIP	RoHS
-40ºC to +125ºC	2 MHz	TK68HC811E2CPBE2	TK7740D	52 PQFP	RoHS

Termination Finish for CDIP Package- RoHS:

Leads are plated with 50-350 u" Ni then plated with 60 u" Min Au Anneal level - annealed after Ni flash applied and after 50-350 u" Ni is applied Minimum Sn thickness - there is no Sn on the package

Contact Information

Please contact orders@tekmos.com for further information.

Tekmos, Inc.
14121 Hwy 290 W.
Bldg 15
Austin, TX 78737
512 342-9871 phone
Sales@Tekmos.Com
www.Tekmos.com

Revision History

Date	Revision	Description
12/19/13	1.0	Initial Release
3/05/14	1.1	Fix Typographical Errors
4/21/14	1.2	Add 175C operation; Delete 52 pin package
6/6/18	1.3	Add 52 pin packages
6/27/18	1.4	Add pinout, ordering information
07/2/18	1.5	Replace LQFP package, with PQFP package
8/23/18	1.6	Added PQFP ordering information
8/28/18	1.7	Updated PQFP temperature range
4/22/20	1.8	Updates PQFP Temperature Range
6/08/20	1.9	Update electrical specifications
6/29/20	1.10	Remove “-“ in part number
6/13/22	1.11	Updated pinlist on PQFP package. Changed Tekmos Contact Address.
5/15/23	1.12	Updated Ordering Information table to include Pb Finish on TK7740E device. Change the lower temp range to -40C for TK7740E device.
8/7/2023	1.13	Updated electrical characteristics to reflect the M68HC11E Freescale Datasheet. Added termination finish to RoHS device.
2/13/2024	1.14	Removed Pb-Finish option on Ordering Information Table.