TK68HC705B
HC7053 Microcontroller with Flash

(v1.0) November 8, 2019 Data Sheet

Features

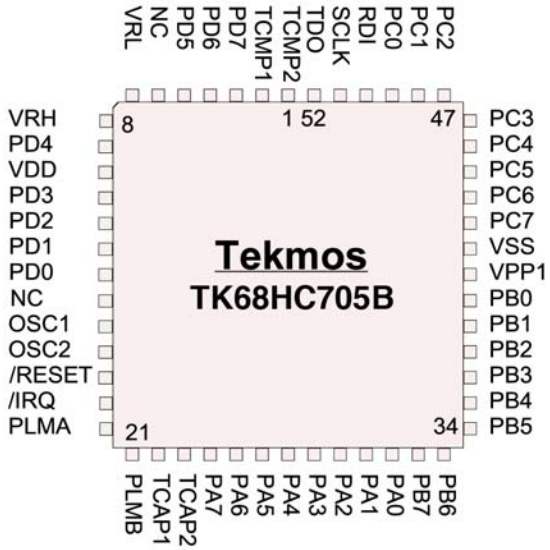
Available in either the 16K or 32K flash memory sizes

- Pin compatible, timing compatible replacement for the industry standard 68HC05 family CPU
- Fully static design supports operation from 0 to 4.2 MHz at 5 volts and 2 MHz at 3 volts
- Embedded memory with:
  - 176 bytes of RAM
  - 16K or 32K bytes of user Flash
  - 256 bytes of byte erasable EEPROM
  - Security bit for 224 bytes of EEPROM
- Advanced peripherals including:
  - Three 8-bit parallel I/O ports
  - One 8-bit input-only port
  - 16-bit timer with 2 input captures and 2 output compares
  - 8-channel, 8-bit A/D converter
  - UART (SCI) with independent baud rate selection and receiver wake up function
  - Watchdog timer
  - 5 Interrupt sources
  - 2 PLM systems for D/A use
- Self test / bootstrap mode
- Multiple power saving modes
- On chip crystal oscillator with divide by 2 or divide by 32 modes
- Optional E-Clock output
- Available in 52-pin PLCC package
- -40 to +85°C operating temperature
- Direct replacement for NXP MC68HC705B16 and MC68HC705B32 microcontrollers

General Description

The TK68HC705B is a derivative of the HC05 microcontroller architecture. With a rich set of RAM, ROM, and EEPROM memory and a full set of peripherals, the TK68HC705B is well suited to a variety of controller tasks. These parts have been designed to be drop-in replacements for the NXP MC68HC705B16 or MC68HC705B32, with identical code execution, pin compatibility, and equivalent timing.

Pin Out



Pin Descriptions

PLCC	Name	Description
1	TCM2	Timer Output Compare Function 2
2	TCMP11	Timer Output Compare Function 1
3	PD7 / AN7	Port D, Bit 7 / ADC Channel 7
4	PD6 AN6	Port D, Bit 6 / ADC Channel 6
5	PD5 / AN5	Port D, Bit 5 / ADC Channel 5
6	NC	No Connect
7	VRL	ADC Voltage Reference Low
8	VRH	ADC Voltage Reference High
9	PD4 / AN4	Port D, Bit 4 / ADC Channel 4
10	VDD	Positive Supply
11	PD3 / AN3	Port D, Bit 3 / ADC Channel 3
12	PD2 / AN2	Port D, Bit 2 / ADC Channel 2
13	PD1 / AN1	Port D, Bit 1 / ADC Channel 1
14	PD0 / AN0	Port D, Bit 0 / ADC Channel 0
15	NC	No Connect
16	OSC1	Crystal Input / External Clock Input
17	OSC2	Crystal Output
18	/RESET	Active low Reset Input
19	/IRQ	Active Low, External Interrupt Input
20	PLMA	Pulse Length Modulator A Output
21	PLMB	Pulse Length Modulator B Output
22	TCAP1	Timer Input Capture 1
23	TCAP2	Timer Input Capture 2
24	PA7	Port A, Bit 7
25	PA6	Port A, Bit 6
26	PA5	Port A, Bit 5
27	PA4	Port A, Bit 4
28	PA3	Port A, Bit 3
29	PA2	Port A, Bit 2
30	PA1	Port A, Bit 1
31	PA0	Port A, Bit 0
32	PB7	Port B, Bit 7
33	PB6	Port B, Bit 6
34	PB5	Port B, Bit 5
35	PB4	Port B, Bit 4
36	PB3	Port B, Bit 3
37	PB2	Port B, Bit 2
38	PB1	Port B, Bit 1
39	PB0	Port B, Bit 0
40	VPP1	EEPROM Charge Pump Output
41	VSS	Ground
42	PC7	Port C, Bit 7
43	PC6	Port C, Bit 6
44	PC5	Port C, Bit 5
45	PC4	Port C, Bit 4
46	PC3	Port C, Bit 3
47	PC2 / ECLK	Port C, Bit 2 / ECLK output
48	PC1	Port C, Bit 1
49	PC0	Port C, Bit 0
50	RDI	SCI Receive Data Input
51	SCLK	SCI Clock Output
52	TDO	SCI Transmit Data Output

Architecture

The TK68HC705B architecture consists of a classic 68HC05 core controller surrounded by 176 bytes of RAM, 5950 bytes of ROM, and 256 bytes of EEPROM. The TK68HC705B also contains a 16-bit timer, a serial port, 4 parallel ports, an A/D converter, a COP watchdog, and a PLM (Pulse Length Modulator).

68HC05 Core

The Tekmos HC05 core, register set, instructions, and timing are the same as in the classic HC05. This allows existing software to run without modification.

Memory

The memory address space of the TK68HC705B is divided up into control registers, RAM, ROM, and EEPROM.

Control Registers

The first 32 bytes of the memory space is allocated to control and status registers. The addresses of these registers and the definitions of the register bits is shown in the register address map.

RAM

The TK68HC705B contains 176 bytes of RAM. This RAM is shared between user variables and the program stack.

FLASH

The TK68HC705B contains 5950 bytes of user Flash. There is a 48 byte page 0 Flash, 5888 bytes of user program Flash, and 14 bytes of user vectors.

EEPROM

The TK68HC705B contains 256 bytes of EEPROM. One byte is used by the options register, and the remaining 255 bytes are for general purpose use.

I/O Ports

The TK68HC705B has 4 8-bit ports. Three ports (A, B, and C) are general purpose I/O ports. The fourth port (D) is an input only port. These pins are also shared with the ADC inputs.

Ports A and B

Each of these ports has a data and a direction register. This allows the direction of each bit to be assigned on a bit-by-bit basis.

Port C

Port C behaves the same as Ports A or B. In addition, bit 2 of Port C can be programmed to output the ECLK signal. This is controlled by the EEPROM / ECLK Control register.

Port D

Port D is an input only port. The Port D pins are shared with the ADC inputs when the ADC has been enabled.

Reading Port D during an ADC cycle may interfere with the accuracy of the measurement. Also, reading analog voltages on the digital inputs may result in greater power dissipation.

Timer

The TK68HC705B has a programmable timer consisting of a divide-by-4 prescaler, a 16-bit free-running timer, and associated input capture / output compare circuitry. The timer is accessed and controlled by 16 registers.

Counter

The heart of the timer is a free-running, 16-bit counter, driven by a divide-by-4 prescaler off of the system clock.

Reading the MSB of the counter latches in the current value of the LSB into a buffer. This allows for an accurate read of the current counter value.

There are two different read locations for the counter. Reading the counter LSB clears the TOF flag. Reading the alternate counter location does not clear the TOF flag.

Timer Control Register

The timer is controlled through a timer control register. This register is at location $0012.

Timer Control Register (TCR)		
Bit	Name	Function
7	ICIE	Input Captures Int. Enable
6	OCIE	Output Compares Int. Enable
5	TOIE	Timer Overflow Int. Enable
4	FOLV2	Force Output Compare 2
3	FOLV1	Force Output Compare 1
2	OLV2	Output Level 2
1	IEDG1	Input Edge 1
0	OLVL1	Output Level 1

ICIE (Bit 7) – Input Captures Interrupt Enable

Setting this bit allows a timer interrupt whenever the ICF1 or ICF2 status flag in the timer status register is set.

OCIE (Bit 6) – Output compares Interrupt Enable

Setting this bit allows a timer interrupt whenever the OCF1 or OCF2 status flags in the timer status register have been set.

TOIE (Bit 5) – Timer Overflow Interrupt Enable

Setting this bit allows a timer interrupt whenever the TOF status flag in the timer status register has been set.

FOLV2 (Bit 4) – Force Output Compare 2

Writing a one to this bit triggers a software force compare to the OLV2 bit. Writing a zero has no effect. This bit always reads a zero.

FOLV1 (Bit 3) – Force Output Compare 1

Writing a one to this bit triggers a software force compare to the OLV1 bit. Writing a zero has no effect. This bit always reads a zero.

OLV2 (Bit 2) – Output Level 2

This bit controls the polarity of the TCMP2 pin after a successful output compare.

IEDGE1 (Bit 1) – Input Edge 1

This bit controls which edge of the TCAP1 pin is used to trigger a transfer of the counter to the input capture register 1. A one in this bit specifies the positive going edge, while a zero specifies the negative going edge.

The TCAP2 register is always configured as negative triggered.

OLV1 (Bit 0) – Output Level 1

This bit controls the polarity of the TCMP1 pin after a successful output compare.

Timer Status Register

The status of the timer is monitored through the timer status register, at location $0013.

Timer Status Register (TSR)		
Bit	Name	Function
7	ICF1	Input Capture Flag 1
6	OCF1	Output Compare Flag 1
5	TOF	Timer Overflow Flag.
4	ICF2	Input Capture Flag 2
3	OCF2	Output Compare Flag 2
2	X	Unused
1	X	Unused
0	X	Unused

ICF1 (Bit 7) – Input Capture Flag 1

The input capture flag 1 is set when the selected edge of the TCAP1 pin is detected. If the ICIE bit is also set, then an interrupt will be generated.

This bit is cleared by reading the TSR register, followed by reading the input capture low register 1.

OCF1 (Bit 6) – Output Compare Flag 1

The output compare flag 1 is set when the counter matches the contents of the output compare register. If the OCIE bit is also set, then an interrupt will be generated.

This bit is cleared by reading the TSR register, and then either reading or writing the output compare 1 low register.

TOF (Bit 5) – Timer Overflow Flag

The timer overflow flag is set when the counter overflows from $FFFF to $0000. If the OIE bit is also set, then an interrupt will be generated.

This bit is cleared by reading the TSR register and then reading the counter low register.

ICF2 (Bit 4) – Input Capture Flag 2

The input capture flag 2 is set when the negative edge of the TCAP2 pin is detected. If the ICIE bit is also set, then an interrupt will be generated.

This bit is cleared by reading the TSR register, followed by reading the input capture low register 2.

OCF2 (Bit 3) – Output Compare Flag 2

The output compare flag 2 is set when the counter matches the contents of the output compare register. If the OCIE bit is also set, then an interrupt will be generated.

This bit is cleared by reading the TSR register, and then either reading or writing the output compare 2 low register.

Input Capture

The input capture mode allows the contents of the counter to be captured (stored) by an external event. This allows for the measurement of the elapsed time of an external event

The TK68HC705B contains two 16-bit input capture registers (ICR1 and ICR2). These registers are read-only, and will contain the counter count + 1 after a valid transition of the TCAP pin.

A capture sets the ICFx bit in the TSR register. If the ICIE bit is also set, then an interrupt will be generated.

Output Compare

The output compare mode compares the contents of the counter with each of two different output compare registers (OCR1 and OCR2). When they match, the OCFx bit is set, and an interrupt is optionally generated. The TCMPx pins are also updated.

Pulse Length Modulation

The timer counters can be used to provide a clock source to the PLM circuitry.

Stop Mode

The timer stops running while the CPU is in the STOP mode. It will be reset if a reset us used to exit the STOP mode.

Wait Mode

The timer is not affected by the wait mode. Any valid timer interrupt will awaken the system.

Serial Port

The serial port, which is also known as a Serial Communications Interface, consists of full-duplex UART with independent transmit and receive baud rate generators. Features include:

- Programmable 8 / 9 bit data length
- Independent baud rate generators
- 32 software selectable baud rates
- Full UART controls
- Flexible interrupt control

The serial port is controlled through a baud rate register, two control registers, and a status register.

Baud Rate Register

The baud rate for the transmitter and receiver are controlled by the Baud Rate Register, at location $000D.

Baud Rate Register (BAUD)		
Bit	Name	Function
7	SCP1	Prescaler Bit 1
6	SCP0	Prescaler Bit 0
5	SCT2	Transmitter Bit 2
4	SCT1	Transmitter Bit 1
3	SCT0	Transmitter Bit 0
2	SCR2	Receiver Bit 2
1	SCR1	Receiver Bit 1
0	SCR0	Receiver Bit 0

SCP1, **SCP0** – Serial Prescaler Select Bits

These two bits select the value of the prescaler divide-by on the internal clock before it is applied to both the transmit and receive baud rate generators.

P1	P0	N
0	0	1
0	1	3
1	0	4
1	1	13

SCT2, **SCT1**, **SCT0** – Transit Baud Rate

These three bits select the divide-by circuit that generates the 16X transmit clock from the prescaler output.

T2	T1	T0	N
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

SCR2, **SCR1**, **SCR0** – Receive Baud Rate

These three bits select the divide-by circuit that generates the 16X transmit clock from the prescaler output.

R2	R1	R0	N
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Serial Communications Control Register 1 (SCCR1)

The Serial Communications Control Register 1 contains control bits covering the 9th bit in data transmission, the wake up modes, and the clocks for synchronous data transmission. This register is located at address $000E.

Serial Communications Control Register 1 (SCCR1)		
Bit	Name	Function
7	R8	Receive Data Bit 8
6	T8	Transmit Data Bit 8
5	X	Unused
4	M	Mode
3	WAKE	Wake-up Mode Select
2	CPOL	Clock Polarity
1	CPHA	Clock Phase
0	LBCL	Last Bit Clock

R8 – Receive Data Bit 8

This bit contains the 9th received data bit when the mode bit M is set for 9-bit operation.

T8 – Transmit Data Bit 8

This bit contains the 9th bit to be transmitted when the mode bit M is set for 9-bit operation.

M – Mode

This bit selects between 8-bit (0) and 9-bit (1) operation.

WAKE – Wake-up Mode Select

When the WAKE bit is set, the receiver will wake-up if the 8th (or 9th if M=1) received bit is set.

If this bit is cleared, then the receiver will wake-up on the 11th (or 12th if M=1) idle bit has been received.

CPOL – Clock Polarity

This bit determines the polarity of the SCLK pin outside of the transmission window. A 1 provides a steady high value.

CPHA – Clock Phase

This bit controls the phase of the SCLK signal with respect to the data. A 1 causes a rising edge at the beginning of the data bit. A 0 causes a rising edge at the middle of a data bit.

LBCL – Last Bit Clock

Setting this bit causes an additional clock for the last bit in synchronous data transmissions.

Serial Communications Control Register 2 (SCCR2)

Individual serial functions are enabled and disabled by the bits in the Serial Communications Control Register 2. This register is located at address $000F.

Serial Communications Control Register 2 (SCCR2)		
Bit	Name	Function
7	TIE	Transmit Interrupt Enable
6	TCIE	Transmit Complete Int. En.
5	RIE	Receive Interrupt Enable
4	ILIE	Idle Line Interrupt Enable
3	TE	Transmit Enable
2	RE	Receive Enable
1	RWU	Receiver Wake-Up
0	SBK	Send Break

TIE – Transmit Interrupt Enable

Setting the TIE bit enables the transmit data register empty interrupt.

TCIE – Transmit Complete Interrupt Enable

Setting the TCIE bit enables the transmit complete interrupt

RIE – Receive Interrupt Enable

Setting the RIE bit enables the receive interrupt.

ILIE – Idle Line Interrupt Enable

Setting the ILIE bit enables the idle line interrupt.

TE – Transmit Enable

Setting the TE bit enables the transmitter.

RE – Receive Enable

Setting the RE bit enables the receiver.

RWU – Receiver Wake-Up

Setting the RWU bit puts the receiver to sleep, and enables the wake-up function.

SBK – Send Break

Setting the SBK bit sends a 10-bit (11 if M=1) 0 string. At the completion of the break, a 1 is sent to insure the correct recognition of the next start bit.

Serial Communications Status Register

The Serial Communications Status Register provides the current status of the SCI. This register is located at $0010.

Serial Communications Status Register (SCSR)		
Bit	Name	Function
7	TDRE	Transmit Data Empty
6	TC	Transmit Complete
5	RDRF	Receive Data Full Flag
4	IDLE	Idle line detected Flag
3	OR	Overrun Error Flag
2	NF	Noise Error Flag
1	FE	Framing Error Flag
0	x	Unused

TDRE – Transmit Data Register Empty Flag

The TDRE bit is set when the contents of the transmit data register are transferred to the transmitter. Reading the SCSR register, followed by a write to the transmit data register clears the TDRE flag. The SCSR register must be read before new data will transfer to the transmitter.

TC – Transmit Complete Flag

The TC bit indicates the current status of the transmitter. It is set when the transmitter and the transmit data register are empty.

RDRF – Receive Data Register Full Flag

The RDRF flag is set when the contents of the receiver are transferred to the receive data register. Any receive errors will also cause the NF bit to be set in the same cycle.

The RDRF flag will be cleared by reading the SCSR register, and then reading the receive data register.

IDLE – Idle Line Detected Flag

The IDLE bit is set when a receiver idle line condition has been detected. An idle line is defined as the receipt of 10/11 consecutive ones.

The idle flag is cleared by a read of the SFSR register, followed by a read of the receive data register.

The IDLE flag will not be set again until a non-idle condition has occurred.

OR – Overrun Error Flag

The OR flag is set when new data is ready to be transferred into the receive data register, and the old data has not been read. The original data remains in the receive data register, and the new data is lost.

The OR flag is cleared by reading the SFSR register, followed by a read of the receive data register.

NF – Noise Error Flag

The NF flag is set if noise is detected on a valid start bit, data bits, or the stop bit. If there was noise, the NF flag will be set at the same time as the RDRF flag.

The NF flag is cleared by reading the SFSR register, followed by a read of the receive data register.

FE – Framing Error Flag

The FE bit is set by receiving a zero in the stop bit position. The presence of the FE inhibits further reception until the FE bit has been cleared. The FE flag is cleared by reading the SFSR register, followed by a read of the receive data register.

Analog to Digital Converter

The TK68HC705B contains an 8-bit analog to digital converter. The converter has a 16:1 analog multiplexor in front of it, and uses an external reference.

The ADC operates off of either the system clock or an internal RC oscillator. When not in use, the ADC may be powered down to save power.

Port D Data Register (PORTD)

Eight of the ADC inputs are shared with the Port D input pins. Reading Port D during an ADC conversion may affect the accuracy of the conversion. This register is located at $0003.

A/D Data Register (ADDATA)

The results of the ADC conversion are in the ADDATA register. This register is located at $0008.

A/D Status and Control Register (ADSTAT)

The ADSTAT register controls the analog to digital converter. It also provides the status for the ADC conversion. The ADSTAT register is located at $0009.

Serial Communications Control Register 2 (SCCR2)		
Bit	Name	Function
7	COCO	Conversion Complete
6	ADRC	ADC RC Oscillator Ctrl
5	ADON	ADC On
4	0	
3	CH3	Channel Select Bit 3
2	CH2	Channel Select Bit 2
1	CH1	Channel Select Bit 1
0	CH0	Channel Select Bit 0

COCO – Conversion Complete

This bit is set when the analog to digital conversion is complete. It is cleared by reading the ADDATA register, or by writing a 0 to this bit.

ADRC – ADC RC Oscillator Control

This bit selects the source of the ADC clock. When set, the ADC runs off of an internal RC oscillator. When cleared, it uses the bus clock.

Selecting the RC oscillator turns on the RC oscillator independently of the ADON bit. This allows the RC oscillator to reach speed and stabilize before it is used by the ADC.

ADON – ADC On

Setting this bit turns on the ADC.

CH3-CH0 – Input Channel Select

These 4 bits control the 16:1 mux on the ADC input. The following table explains which input is selected.

ADC Multiplexer Selection	
CH3-CH0	Input
0	AN0
1	AN1
2	AN2
3	AN3
4	AN4
5	AN5
6	AN6
7	AN7
8	VRH
9	(VRH + VRL) / 2
10	VRL
11	VRL
12	VRL
13	VRL
14	VRL
15	VRL

COP Watchdog

The TK68HC705B contains a Computer Operating Properly (COP) watchdog circuit. This can be enabled automatically after reset, or it can be enabled by software by writing to the WDOG bit in the Miscellaneous register. Once enabled, the watchdog cannot be disabled by software.

In the COP Watchdog circuit, bit 7 of the free-running counter is used as a clock for an 8-bit watchdog counter. Should this register ever overflow, it will drive the reset pin low, which will trigger a system reset.

Writing a 1 to the WDOG bit will clear the watchdog counter.

If the watchdog is running, the STOP instruction will be inhibited. Instead, the STOP instruction causes an immediate watchdog timeout and system reset.

A mask option controls the state of the watchdog during the WAIT mode. This allows selection of either normal operation or a halt of the watchdog counter during WAIT.

Pulse Length Modulator

The TK68HC705B contains two pulse length modulators (PLM). These are known as A and B.

Each PLM has a data register that contains the pulse length value. The “A” register PLMA is located at $000A, and the “B” register is located at $000B.

The data registers are double buffered, so that they can be changed without introducing intermediate errors on the outputs.

Writing a $00 to the data register produces an output that is always low. Writing a $80 produces a 50% duty cycle. Writing a $FF produces a 255 / 256 duty cycle.

The outputs of each PLM are connected to the external pins PLMA and PLMB.

Miscellaneous Register

The miscellaneous register contains 3 control bits for the PLM circuit. It also contains control bits for the interrupt controller and the watchdog timer. The miscellaneous register is at $000C.

Miscellaneous (MISC)		
Bit	Name	Function
7	POR	Power-On-Reset
6	INTP	Interrupt on Positive Edge
5	INTN	Interrupt on Negative Edge
4	INTE	External Interrupt Enable
3	SFA	Slow or Fast for PLMA
2	SFB	Slow or Fast for PLMB
1	SM	Slow Mode
0	WDOG	Watchdog Control

POR – Power-On-Reset

The POR flag is set when the part first powers up. It may be used by software to determine the source of a reset.

This bit may be cleared by writing a zero to it.

INTP – Interrupt on Positive Edge
INTN – Interrupt on Negative Edge

These two bits determine the external interrupt sensitivity options.

External Interrupt Options		
INTP	INTN	Option
0	0	Negative Edge and Low Level
0	1	Negative Edge Only
1	0	Positive Edge Only
1	1	Both Edges

INTE – External Interrupt Enable

Setting the INTE bit enables external Interrupts

SFA – Slow or Fast for PLMA
SFB – Slow or Fast for PLMB

These two bits control the clock source for each PLM. A 1 uses a clock of 4096 * timer clock period. A 0 uses a clock of 256 * timer clock period.

SM – Slow Mode

Setting this bit causes the system to run 16 times slower than normal.

WDOG – Watchdog Control

Writing a 1 to the WDOG bit both enables the watchdog counter and clears the watchdog counter. Once enabled, the watchdog cannot be disabled except through a reset.

Interrupts

The TK68HC705B contains a multiple source interrupt capability. When an interrupt occurs, the processor sets the interrupt mask bit to prevent future interrupts, saves the register contents on the stack, fetches the interrupt vector, and calls that location.

Executing the return from interrupt instruction (RTI) restores the registers and resumes normal processing.

When multiple events request an interrupt at the same time, the processor decides upon which interrupt to service based on a fixed priority structure.

Interrupt Priorities		
Priority	Source	Vector
1	Reset	$1FFE / F
2	Software	$1FFC / D
3	External	$1FFA / B
4	Timer input capture	$1FF8 / 9
5	Timer output compare	$1FF6 / 7
6	Timer overflow	$1FF4 / 5
7	Serial	$1FF2 / 3

EEPROM

The TK68HC705B contains a 256 byte general purpose EEPROM. This is located between addresses $0100 and $01FF. The chip creates its own programming voltage, which may be observed on the VPP1 pin. This pin should be left open.

The EPROM is controlled through the EEPROM control register, which is located at address $0007.

EEPROM Control Register		
Bit	Name	Function
7	0	
6	0	
5	0	
4	0	
3	ECLK	
2	E1ERA	EEPROM Erase
1	E1LAT	EEPROM Latch Enable
0	E1PGM	EEPROM Charge Pump

ECLK – External Clock Output Enable

Setting this bit allows the ECLK CPU clock to be output on the PC2 pin. When clear, the PC2 acts as a normal port pin.

E1ERA – EEPROM Erase / Program

If the E1LAT and E1PGM bits are set, then this bit selects whether an erase (1) or a programming (0) operation will occur.

E1LAT – EEPROM Programming Latch Enable

Setting this bit allows EEPROM address and data to be latched into the EEPROM for program or erase functions. Clearing this bit allows for normal read operations. Clearing this bit also forces the E1ERA and E1PGM bits to zero.

E1PGM – EEPROM Charge Pump Enable

Setting this bit turns on the internal charge pump. Clearing the bit turns off the charge pump.

Register Address Map

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000h	Port A Data	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
0001h	Port B Data	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0002h	Port C Data	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
0003h	Port D Input Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
0004h	Port A Data Direction	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
0005h	Port B Data Direction	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
0006h	Port C Data Direction	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
0007h	EEPROM / ECLK Control	0	0	0	0	ECLK	E1ERA	E1LAT	E1PGM
0008h	A/D Data								
0009h	A/D Status / Control	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0
000Ah	Pulse Length Modulation A								
000Bh	Pulse Length Modulation B								
000Ch	Miscellaneous	POR	INTP	INTN	INTE	SFA	SFB	SM	WDOG
000Dh	SCI Baud Rate	SCP1	SCP0	SCT2	SCT1	SCT0	SCR2	SCR1	SCR0
000Eh	SCI Control 1	R8	T8	X	M	WAKE	CPOL	CPHA	LBCL
000Fh	SCI Control 2	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
0010h	SCI Status	TDRE	TC	RDRF	IDLE	OR	NF	FE	x
0011h	SCI Data								
0012h	Timer Control	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1
0013h	Timer Status	ICF1	OCF1	TOF	ICF2	OCF2	x	x	x
0014h	Capture High 1								
0015h	Capture Low 1								
0016h	Compare High 1								
0017h	Compare Low 1								
0018h	Counter High								
0019h	Counter Low								
001Ah	Alternate Counter High								
001Bh	Alternate Counter Low								
001Ch	Capture High 2								
001Dh	Capture Low 2								
001Eh	Compare High 2								
001Fh	Compare Low 2								

Electrical Specifications

Maximum Ratings

Characteristics		Symbol	Min	Max	Unit
Supply Voltage (1)		Vdd	-0.5	5.5	V
Input Voltage (Except Vpp1)		Vin	Vss – 0.3	Vdd + 0.3	V
Input Voltage – IRQ pin only		Vin	Vss – 0.3	2 * Vdd	V
Operating Temperature Range	Commercial	Tac	0	70	°C
	Industrial	Tai	-40	85	°C
	Military	Tam	-55	125	°C
Storage Temperature range		Tstg	-65	+150	°C
Current Drain Per Pin (2)					
- Source		Id		25	mA
- Sink		Is		45	mA

Notes for Maximum Ratings:

1. All voltages are respect to Vss.
2. The maximum current drain per pin is for one pin at a time.

Note:

This device contains circuitry that is designed to protect against accidental ESD damage or electrical overstress. However, it is recommended that the customer take precautions to insure that voltages higher than Vdd are not applied to this circuit. Unused inputs should be connected to either Vss or Vdd.

DC Electrical Specifications (V_{DD} = 5.0 V +/- 10%, V_{SS} = 0 V)

Characteristics (1)	Condition	Symbol	Min	Max	Unit
Output Voltage	Ioh= -10 uA Iol = 10 uA	V_{OH} V_{OL}	Vdd-0.1	 0.1	V V
Output High Voltage PA0-7, PB0-7, PC0-7, TCMP1, TCMP2 TDO, SCK, PLMA, PLMB	 Ioh = 0.8 mA Ioh = 1.6 mA	 V_{OH} V_{OH}	 Vdd – 0.8 Vdd – 0.8	 Vdd Vdd	 V V
Output Low Voltage PA0-7, PB0-7, PC0-7, TCMP1, TCMP2 TDO, SCK, PLMA, PLMB /RESET	 Iol = 1.6 mA Iol = 1.6 mA Iol = 1.6 mA	 V_{OL} V_{OL} V_{OL}	 0 0 0	 0.4 0.4 1.0	 V V V
Input High Voltage PA0-7, PB0-7, PC0-7, PD0-7, OSCI /IRQ, /RESET, TCAP1, TCAP2, RDI		V_{IL}	0.7 * Vdd	Vdd	V
Input Low Voltage PA0-7, PB0-7, PC0-7, PD0-7, OSCI /IRQ, /RESET, TCAP1, TCAP2, RDI		V_{IL}	0.0	0.2 * Vdd	V
Supply Current (3) RUN (SM=0) RUN (SM=1) WAIT (SM=0) WAIT (SM=1) STOP 0 to 70 (Commercial) -40 to 85 (Industrial) -55 to 125 (Military)		 I_{OD}		 6 1.5 2 1 10 20 60	 mA mA mA mA uA uA uA
High-Z Leakage Current PA0-7, PB0-7, PC0-7, TDO, RESET, SCLK		I_{IL}		 1	 uA
Input Current (-40°C to +85°C) /IRQ, OSC1, TCAP1, TCAP2, RDL, PD0-7		I_{IN}		 1	 uA
Input Current (-55°C to 125 °C) /IRQ, OSC1, TCAP1, TCAP2, RDL		I_{IN}		 5	 uA
Capacitance Ports, /RESET, TDO, SCLK /IRQ, TCAP1, TCAP2, OSC1, RDI PDO-7 (A/D Off) PD0-7 (A/D On)	 Typical (2) Typical	 C_{OUT} C_{IN} C_{IN} C_{IN}	 	 12 8 12* 22*	 pF

Notes for DC Characteristics:

1. Idd measurements are taken with decoupling capacitors across the supply. This produces an average value rather than a peak value.
2. Typical measurements are defined at 5 volts and 25°C.
3. The Idd measurement for RUN and WAIT is made with a 4.2 MHz square wave clock source, all inputs within 0.2V to the supply, no DC loads, and with a 50 pF load on every output and 20 pF on OSC2.

   The Idd for STOP and WAIT has all ports as inputs, all inputs 0.2 volts away from the supply.

   The STOP Idd is measured with OSC1 = Vdd.

3.3 Volt A/D Characteristics (V_{DD} = 3.3 V +/- 10%, V_{SS} = 0 V)

Characteristics (1)	Condition	Symbol	Min	Max	Unit
Output Voltage	Ioh= -10 uA Iol = 10 uA	V_{OH} V_{OL}	Vdd-0.1	 0.1	V V
Output High Voltage PA0-7, PB0-7, PC0-7, TCMP1, TCMP2 TDO, SCK, PLMA, PLMB	 Ioh = 0.2 mA Ioh = 0.4 mA	 V_{OH} V_{OH}	 Vdd – 0.3 Vdd – 0.3	 Vdd Vdd	 V V
Output Low Voltage PA0-7, PB0-7, PC0-7, TCMP1, TCMP2 TDO, SCK, PLMA, PLMB /RESET	 Iol = 0.4 mA Iol = 0.4 mA Iol = 0.4 mA	 V_{OL} V_{OL} V_{OL}	 0 0 0	 0.3 0.3 0.6	 V V V
Input High Voltage PA0-7, PB0-7, PC0-7, PD0-7, OSCI /IRQ, RESET, TCAP1, TCAP2, RDI		V_{IL}	0.7 * Vdd	Vdd	V
Input Low Voltage PA0-7, PB0-7, PC0-7, PD0-7, OSCI /IRQ, /RESET, TCAP1, TCAP2, RDI		V_{IL}	0.0	0.2 * Vdd	V
Supply Current (3) RUN (SM=0) RUN (SM=1) WAIT (SM=0) WAIT (SM=1) STOP 0 to 70 (Commercial) -40 to 85 (Industrial) -55 to 125 (Military)		 I_{OD}		 3 1 1.5 0.5 10 10 40	 mA mA mA mA uA uA uA
High-Z Leakage Current PA0-7, PB0-7, PC0-7, TDO, RESET, SCLK		I_{IL}		 1	 uA
Input Current (0-70) /IRQ, OSC1, TCAP1, TCAP2, RDL, PD0-7		I_{IN}		 1	 mA
Input Current (-55 to 125) /IRQ, OSC1, TCAP1, TCAP2, RDL		I_{IN}		 5	 uA
Capacitance Ports, /RESET, TDO, SCLK /IRQ, TCAP1, TCAP2, OSC1, RDI PDO-7 (A/D Off) PD0-7 (A/D On)	 Typical (2) Typical	 C_{OUT} C_{IN} C_{IN} C_{IN}		 12 8 12* 22*	 pF

Notes for DC Characteristics:

1. Idd measurements are taken with decoupling capacitors across the supply. This produces an average value rather than a peak value.
2. The Idd measurement for RUN and WAIT is made with a 2.0 MHz square wave clock source, all inputs within 0.2V to the supply, no DC loads, and with a 50 pF load on every output and 20 pF on OSC2.

   The Idd for STOP and WAIT has all ports as inputs, all inputs 0.2 volts away from the supply.

   The STOP Idd is measured with OSC1 = Vdd.

   The WAIT Idd is linearly proportional to the OSC2 capacitance.

5 Volt A/D Characteristics (V_{DD} = 5.0 V +/- 10%, V_{SS} = 0 V)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits in the A/D	8		Bit
Non-Linearity	Maximum deviation from the best straight line through the A/D transfer characteristics. VRH = Vdd and VRL = 0V		+/- 0.5	LSB
Quantization Error	Uncertainty due to converter resolution		+/- 0.5	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary output code for all errors		1	LSB
Conversion Range	The analog input voltage range	VRL	VRH	V
VRH	Maximum analog reference voltage	VRL	Vdd + 0.1	V
VRL	Minimum analog reference voltage	Vss – 0.1	VRH	V
Delta VR (1)	Minimum voltage difference between VRH and VRL	3		V
Conversion Time	Total time to perform an A/D conversion External clock Internal RC oscillator		 32 32	 tCYC uS
Monotonicity	Conversion result never decreases with increasing voltage, and result never has missing codes	Guaranteed		pF
Zero Input Reading	Conversion result with VIN = VRL.	00		Hex
Full Scale Reading	Conversion result with VIN = VRH		FF	Hex
Sample Acquisition Time	Analog input acquisition sampling External clock Internal RC oscillator (2)		 12 12	 tCYC uS
Sample / Hold Capacitance	Input Capacitance on PD0–7		12	pF
Input Leakage (3)	Input Leakage on A/D pins PD0–7		1	uA

Notes for 5 Volt A/D Characteristics:

1. Accuracy is tested and guaranteed at Delta VR = 5V. The performance is verified down to 2.5V.
2. Source impedances of greater than 10K ohms will affect the internal charging time, and thus the accuracy.
3. The input leakage current, flowing through the source impedance can introduce errors in the A/D measurement.

3.3 Volt A/D Characteristics (V_{DD} = 3.3 V +/- 10%, V_{SS} = 0 V)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits in the A/D	8		Bit
Non-Linearity	Maximum deviation from the best straight line through the A/D transfer characteristics. VRH = Vdd and VRL = 0V.		+/- 1.0	LSB
Quantization Error	Uncertainty due to converter resolution		+/- 1.0	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary output code for all errors		+/- 2	LSB
Conversion Range	The analog input voltage range	VRL	VRH	V
VRH	Maximum analog reference voltage	VRL	Vdd + 0.1	V
VRL	Minimum analog reference voltage	Vss – 0.1	VRH	V
Delta VR (1)	Minimum voltage difference between VRH and VRL	3		V
Conversion Time	Total time to perform an A/D conversion External clock Internal RC oscillator		 32 32	 tCYC uS
Monotonicity	Conversion result never decreases with increasing voltage, and result never has missing codes.	Guaranteed		
Zero Input Reading	Conversion result with VIN = VRL	00		Hex
Full Scale Reading	Conversion result with VIN = VRH		FF	Hex
Sample Acquisition Time	Analog input acquisition sampling External clock Internal RC oscillator (2)		 12 12	 tCYC uS
Sample / Hold Capacitance	Input Capacitance on PD0–7		12	pF
Input Leakage (3)	Input Leakage on A/D pins PD0–7		1	uA

Notes for 3.3 Volt A/D Characteristics:

1. Accuracy is tested and guaranteed at Delta VR = 5V. The performance is verified down to Delta 2.5V.
2. Source impedances of greater than 10K ohms will affect the internal charging time, and thus the accuracy.
3. The input leakage current, flowing through the source impedance can introduce errors in the A/D measurement.

5 Volt AC Electrical Specifications (V_{DD} = 5.0 V +/- 10%, V_{SS} = 0 V, Ta = -40ºC to +85ºC)

Characteristics	Symbol	Min	Max	Unit
Oscillator Frequency				
Crystal	F_{OSC}	-	4.2	MHz
External Clock	F_{OSC}	DC	4.2	MHz
Internal Operating Frequency				
Crystal	F_{OP}	DC	2.1	MHz
External Clock	F_{OP}	DC	2.1	MHz
Cycle Time	T_{Cyc}	476	-	ns
Crystal Oscillator Start-up Time	T_{OXOV}		100	ms
Stop Recovery Start-up Time	T_{ILCH}		100	ms
RC Oscillator Stabilization Time	T_{ADRC}		5	us
A/D Converter Stabilization Time	T_{ADON}		500	us
External RESET Input Pulse Width	T_{RL}	1.5		T_{CYC}
Power-On RESET output Pulse Width				
4064 Cycle	T_{PORL}	4064	-	T_{CYC}
16 Cycle	T_{PORL}	16	-	T_{CYC}
Watchdog RESET Output Pulse Width	T_{DOGL}	1.5	-	T_{CYC}
Watchdog Time-Out	T_{DOG}	6144	7168	T_{CYC}
EEPROM Byte Erase Time				
0 to 70 (Commercial)	T_{ERA}	10	-	ms
-40 to 85 (Industrial)	T_{ERA}	10	-	ms
-55 to 125 (Military)	T_{ERA}	10	-	ms
EEPROM Byte Program Time (1)				
0 to 70 (Commercial)	T_{PROG}	10	-	ms
-40 to 85 (Industrial)	T_{PROG}	10	-	ms
-55 to 125 (Military)	T_{PROG}	20	-	ms
Timer				
Resolution (2)	T_{RESL}	4	-	T_{CYC}
Input Capture Pulse Width	T_{THTL}	125	-	ns
Input Capture Pulse Period	T_{TLTL}	See note 3	-	T_{CYC}
Interrupt Pulse Width – Edge Triggered Mode	T_{ILIH}	125	-	ns
Interrupt Pulse Period	T_{ILIL}	See note 4	-	T_{CYC}
OSC1 Pulse Width (5)	T_{OH}, T_{OL}	90	-	ns
Write / Erase Endurance (6)		10000		cycles
Data Retention (6)		10		years

Notes for 5 Volt AC Electrical Specifications:

1. The internal RC oscillator should be used to program the EEPROM when the internal bus frequency is less than 2 MHz.
2. The resolution is set by the 2 bit timer prescaler.
3. The minimum period should be greater than 24 T_{CYC} plus the number of cycles required to execute the capture interrupt service routine.
4. The minimum interrupt period should be greater than 21 T_{CYC} plus the number of cycles required to execute the interrupt service routine.
5. T_{OH} plus T_{OL} should be greater than 238 ns.
6. Temperature = 85°C.

3.3 Volt AC Electrical Specifications (V_{DD} = 3.3 V +/- 10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Characteristics	Symbol	Min	Max	Unit
Oscillator Frequency				
Crystal	F_{OSC}	-	2.0	MHz
External Clock	F_{OSC}	DC	2.0	MHz
Internal Operating Frequency				
Crystal	F_{OP}	DC	1.0	MHz
External Clock	F_{OP}	DC	1.0	MHz
Cycle Time	T_{Cyc}	1000	-	ns
Crystal Oscillator Start-up Time	T_{OXOV}		100	ms
Stop Recovery Start-up Time	T_{ILCH}		100	ms
RC Oscillator Stabilization Time	T_{ADRC}		5	us
A/D Converter Stabilization Time	T_{ADON}		500	us
External RESET Input Pulse Width	T_{RL}	1.5		T_{CYC}
Power-On RESET output Pulse Width				
4064 Cycle	T_{PORL}	4064	-	T_{CYC}
16 Cycle	T_{PORL}	16	-	T_{CYC}
Watchdog RESET Output Pulse Width	T_{DOGL}	1.5	-	T_{CYC}
Watchdog Time-Out	T_{DOG}	6144	7168	T_{CYC}
EEPROM Byte Erase Time				
0 to 70 (Commercial)	T_{ERA}	30	-	ms
-40 to 85 (Industrial)	T_{ERA}	30	-	ms
-55 to 125 (Military)	T_{ERA}	30	-	ms
EEPROM Byte Program Time (1)				
0 to 70 (Commercial)	T_{PROG}	30	-	ms
-40 to 85 (Industrial)	T_{PROG}	30	-	ms
-55 to 125 (Military)	T_{PROG}	30	-	ms
Timer				
Resolution (2)	T_{RESL}	4	-	T_{CYC}
Input Capture Pulse Width	T_{THTL}	250	-	ns
Input Capture Pulse Period	T_{TLTL}	See note 3	-	T_{CYC}
Interrupt Pulse Width – Edge Triggered Mode	T_{ILIH}	125	-	ns
Interrupt Pulse Period	T_{ILIL}	See note 4	-	T_{CYC}
OSC1 Pulse Width (5)	T_{OH}, T_{OL}	200	-	ns
Write / Erase Endurance (6)		10000		cycles
Data Retention (6)		10		years

Notes for 3.3 Volt AC Electrical Specifications:

1. The internal RC oscillator should be used to program the EEPROM when the internal bus frequency is less than 2 MHz.
2. The resolution is set by the 2 bit timer prescaler.
3. The minimum period should be greater than 24 T_{CYC} plus the number of cycles required to execute the capture interrupt service routine.
4. The minimum interrupt period should be greater than 21 T_{CYC} plus the number of cycles required to execute the interrupt service routine.
5. T_{OH} plus T_{OL} should be greater than 500 ns.
6. Temperature = 85°C.

Programming Code

The TK68HC705B series has either a 16K or 32K internal flash memory for program storage. Customers can either provide their program to Tekmos in a MCS or S19 format for programming. Alternately, Tekmos sells a device programmer that customers can use to program the parts themselves.

Because the Tekmos part uses Flash instead of the EPROM used by NXP, the Tekmos part will NOT work in most programmers. An attempt to program the part in a NXP programmer will result in an 18 volt signal being applied to the Tekmos part, which will cause severe damage to the Tekmos part.

Ordering Information

Code	Temperature	Package	Replaces
TK68HC705B16NCFNE	0 to +70	Plastic 52 PLCC	MC68HC05B16FNE
TK68HC705B16NCFNE	-40 to +85	Plastic 52 PLCC	MC68HC05B16CFNE
TK68HC705B16NMFME	-55 to +125	Plastic 52 PLCC	MC68HC05B16MFNE
TK68HC705B32CFNE	0 to +70	Plastic 52 PLCC	MC68HC05B32FNE
TK68HC705B32CFNE	-40 to +85	Plastic 52 PLCC	MC68HC05B32CFNE
TK68HC705B32MFME	-55 to +125	Plastic 52 PLCC	MC68HC05B32

Note: Tekmos does not make a separate part for the 0 to 70 degrees commercial temperature range, When replacing a part originally designed for the commercial temperature range, use the Tekmos part designed for the -40 to +70 industrial temperature range.

Packages are fully RoHS compliant.

Contact Information

The TK68HC705B may be ordered directly from Tekmos

512-342-9871 phone
Sales@Tekmos.com
www.Tekmos.com

Revision History

Date	Revision	Description
7/14/16	1.0	Initial release